EE 3101 Notebook

Fall 2012

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Section 005
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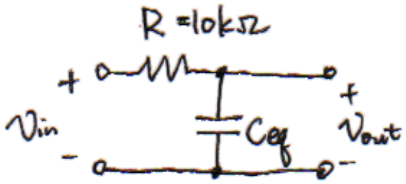
09/11/12 & 09/18/12

Experiment #1 Frequency Response and Filters

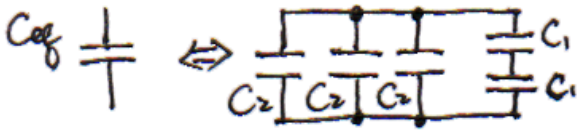
1. Design and construct a RC circuit to implement a low pass filter shown below. Choose component values to make the corner frequency $f_0 = 2kHz$ and the high frequency input impedance $Z_h = 10k\Omega$.



Calculation: We have $Z = R + \frac{1}{sC}$ and for high frequency signal, $Z_h \approx R$. Thus we choose $R = 10k\Omega$.

From $\left|\frac{V_{out}}{V_{in}}\right| = \frac{\frac{1}{sC}}{R+\frac{1}{sC}} = \frac{1}{1+sRC}$, it is obvious to find that $\omega_0 = RC$ and so $f_0 = \frac{1}{2\pi\omega_0} = \frac{1}{2\pi RC}$. Hence, $C = \frac{1}{2\pi R f_0} = \frac{1}{2\pi \times 10k\Omega \times 2kHz} \approx 7.96nF$.

Since capacitor with $7.96nF$ is hard to find, it is safe to choose a very close value $C \cong 8nF$. This is implemented by $C_{eq} = \frac{C_1}{2} + 3C_2$, where $C_1 = 0.01\mu F$ and $C_2 = 0.001\mu F$. The implemented C_{eq} is shown below:

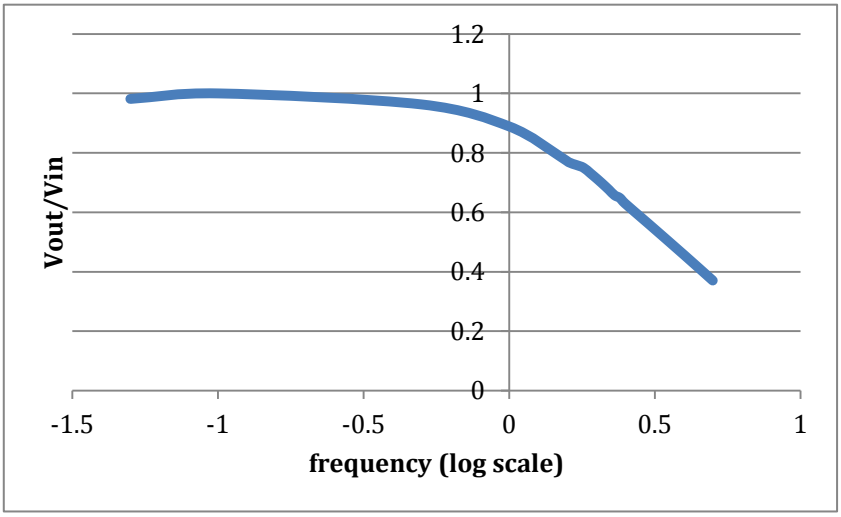


Next is to measure the magnitude and phase of the output as the input signal frequency varies over a wide range, and then determine f where $\left|\frac{V_{out}}{V_{in}}\right| = 0.707$ and where the phase shifted by $45°$ with respect to the input.

The measured results are shown below:

f	V_{in}	V_{out}	V_{out}/V_{in}	ϕ
0.05 kHz	4.32 V	4.24 V	0.981 V/V	−1.44
0.10 kHz	4.32 V	4.32 V	1.000 V/V	2.87
0.50 kHz	4.32 V	4.16 V	0.963 V/V	13.70
1.00 kHz	4.32 V	3.84 V	0.889 V/V	25.10
1.50 kHz	4.32 V	3.40 V	0.787 V/V	36.20
1.60 kHz	4.32 V	3.32 V	0.769 V/V	37.50
1.70 kHz	4.32 V	3.28 V	0.759 V/V	41.60
1.80 kHz	4.32 V	3.24 V	0.750 V/V	42.20
1.90 kHz	4.32 V	3.16 V	0.731 V/V	42.70
2.00 kHz	4.32 V	3.08 V	0.713 V/V	44.60
2.05 kHz	4.32 V	3.04 V	0.704 V/V	45.80

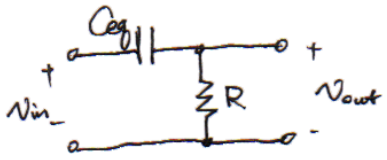
2.10 kHz	4.32 V	3.00 V	0.694 V/V	46.00
2.20 kHz	4.32 V	2.92 V	0.676 V/V	47.00
2.30 kHz	4.32 V	2.84 V	0.657 V/V	48.10
2.40 kHz	4.32 V	2.80 V	0.648 V/V	50.10
2.50 kHz	4.32 V	2.72 V	0.630 V/V	51.20
3.00 kHz	4.48 V	2.52 V	0.563 V/V	57.60
4.00 kHz	4.48 V	2.04 V	0.455 V/V	61.80
5.00 kHz	4.48 V	1.66 V	0.371 V/V	69.50



From the result, it is determined that at around $2.05kHz$, the frequency magnitude is down to 0.707 of its frequency independent value. Also, $f = 2.05kHz$ is where the output is phase shifted by 45 degrees with respect to the input.

Conclusion: What is determined is very reasonable. Since the capacitance has a 0.5% difference and the actual equivalent capacitance measured by the multimeter is around $7.7nF$, the corner frequency is reasonably increased by 2.5%.

2. Interchange the position of the resistor and capacitor in previous problem, and thus the circuit implements a high pass filter now. Similar determination and measurements should be performed. The circuit is shown below:



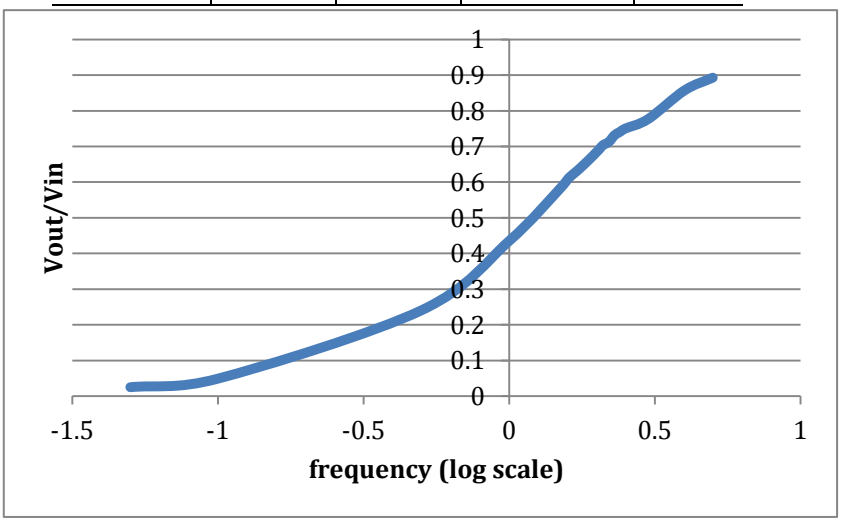
Calculation: It is not hard to find the expression $\left|\frac{V_{out}}{V_{in}}\right| = \frac{R}{R+\frac{1}{sC}} = \frac{sRC}{1+sRC}$.

Once again, the $f_0 = \frac{1}{2\pi\omega_0} = \frac{1}{2\pi RC} \approx 2kHz$.

The measured results are shown below:

f	V_{in}	V_{out}	V_{out}/V_{in}	ϕ
0.05 kHz	4.32 V	0.11 V	0.025 V/V	90.70
0.10 kHz	4.32 V	0.21 V	0.049 V/V	87.80
0.50 kHz	4.32 V	1.04 V	0.241 V/V	76.50

1.00 kHz	4.32 V	1.88 V	0.435 V/V	64.90
1.50 kHz	4.32 V	2.52 V	0.583 V/V	52.40
1.60 kHz	4.32 V	2.64 V	0.611 V/V	50.70
1.70 kHz	4.32 V	2.72 V	0.630 V/V	50.10
1.80 kHz	4.32 V	2.80 V	0.648 V/V	48.50
1.90 kHz	4.32 V	2.88 V	0.667 V/V	46.50
2.00 kHz	4.32 V	2.96 V	0.685 V/V	46.00
2.05 kHz	4.32 V	3.00 V	0.694 V/V	45.30
2.10 kHz	4.32 V	3.04 V	0.704 V/V	44.70
2.20 kHz	4.32 V	3.08 V	0.713 V/V	43.10
2.30 kHz	4.32 V	3.16 V	0.731 V/V	41.40
2.40 kHz	4.32 V	3.20 V	0.741 V/V	40.30
2.50 kHz	4.32 V	3.24 V	0.750 V/V	39.50
3.00 kHz	4.48 V	3.48 V	0.777 V/V	34.60
4.00 kHz	4.48 V	3.84 V	0.857 V/V	27.70
5.00 kHz	4.48 V	4.00 V	0.893 V/V	22.80

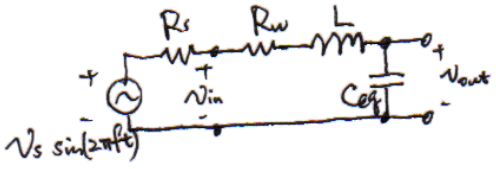


The frequency f, which is about 0.707 of its frequency independent value, falls under the range from 2.1kHz to 2.2kHz. And $2.05kHz \leq f \leq 2.1kHz$ is where the output is phase shifted by 45°.

Conclusion: The result is under the expectation. The measured cutoff frequency has a 5% difference from the calculated value. The reason might be a problem of the actual capacitance $7.7nF$ measured by the multimeter.

3. Design and construct a RLC circuits implementing a low pass filter. The required cutoff frequency is $2kHz$ and a $10mH$ inductor should be used. Measure the frequency response and then use the results to determine the resonant frequency and the *Q*-factor of the circuit.

The circuit is shown below:



Calculation: We know that $f_o = \frac{1}{2\pi\sqrt{LC}} \Rightarrow C = \left(\frac{1}{2\pi f_o}\right)^2 \frac{1}{L} \approx 0.0633\mu F$.

We also know $\left|\frac{V_{out}}{V_{in}}\right| = \frac{1}{\sqrt{\left(1-\left(\frac{\omega}{\omega_o}\right)^2\right)^2 + \left(\frac{\omega}{\omega_o}\right)^2 Q^{-2}}}$. Once we choose $\omega = \omega_o$, and measured V_{out} and V_{in}, it is not hard to determine $Q = \left|\frac{V_{out}}{V_{in}}\right|$.

With the equation $Q = \frac{2\pi f_o L}{R_w}$, we can then also find the R_w by $\frac{2\pi f_o L}{Q}$.

The capacitor with $0.0633\mu F$ is still hard to find. It is reasonable to approximate the capacitance with $0.063\mu F$ so that we can do an implementation. $C_{eq} = \frac{C_1}{2} + C_2 + 3C_3$, where $C_1 = 0.1\mu F$, $C_2 = 0.01\mu F$, and $C_3 = 0.001\mu F$. The implemented C_{eq} is shown below:

The measured result is shown below:

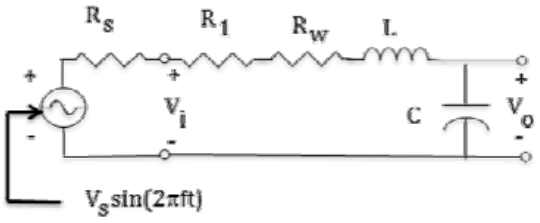
$f = 2kHz = f_o \equiv$ resonant frequency

$V_{in} = 3.6V$

$V_{out} = 15.2V$

Thus we can get $\left|\frac{V_{out}}{V_{in}}\right| \approx 4.2V/V = Q$. And thus the wire resistance is $R_w = \frac{2\pi f_o L}{Q} \approx 0.3k\Omega$.

4. Put a resistor R_1 in series with the inductor so that $Q = 1$. Then measure the frequency response from 200Hz to 20kHz. Compare the result with that of part 1 by plots. The circuit is shown below:

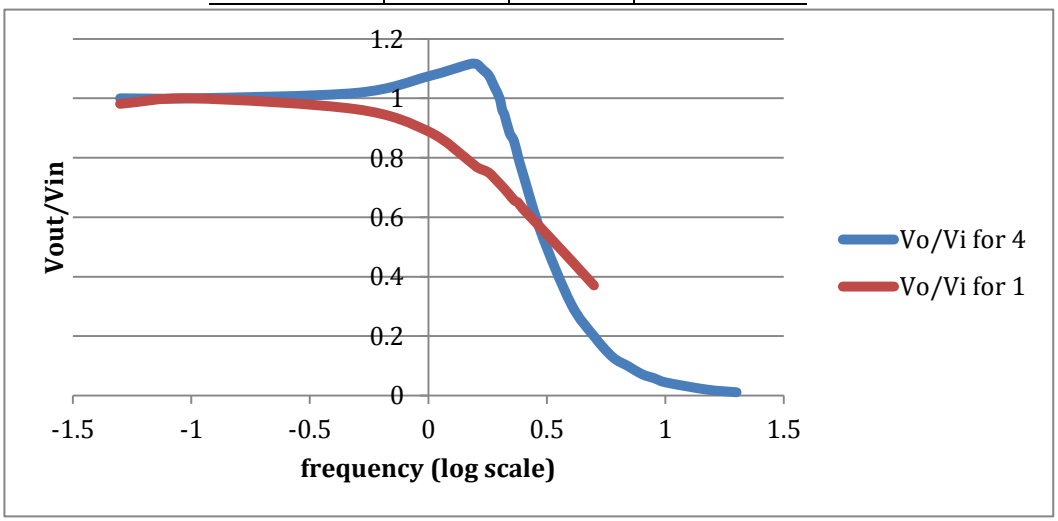


Calculation: $Q = 1 = \frac{2\pi f_o L}{R_w + R_1} \Rightarrow R_1 = 2\pi f_o L - R_w \approx 0.957k\Omega \cong 1k\Omega$.

The measured result is shown below:

f	V_{in}	V_{out}	V_{out}/V_{in}
0.05 kHz	4.32 V	4.32 V	1.000 V/V
0.10 kHz	4.32 V	4.32 V	1.000 V/V
0.50 kHz	4.32 V	4.40 V	1.019 V/V
1.00 kHz	4.32 V	4.64 V	1.074 V/V
1.50 kHz	4.16 V	4.64 V	1.115 V/V
1.60 kHz	4.16 V	4.64 V	1.115 V/V
1.70 kHz	4.16 V	4.56 V	1.096 V/V

1.80 kHz	4.16 V	4.48 V	1.077 V/V
1.90 kHz	4.16 V	4.32 V	1.038 V/V
2.00 kHz	4.16 V	4.16 V	1.000 V/V
2.05 kHz	4.16 V	4.00 V	0.962 V/V
2.10 kHz	4.16 V	3.92 V	0.942 V/V
2.20 kHz	4.16 V	3.68 V	0.885 V/V
2.30 kHz	4.16 V	3.56 V	0.856 V/V
2.40 kHz	4.16 V	3.32 V	0.798 V/V
2.50 kHz	4.16 V	3.12 V	0.750 V/V
3.00 kHz	4.40 V	2.40 V	0.545 V/V
4.00 kHz	4.40 V	1.36 V	0.309 V/V
5.00 kHz	4.40 V	0.88 V	0.200 V/V
6.00 kHz	4.48 V	0.58 V	0.129 V/V
7.00 kHz	4.48 V	0.44 V	0.098 V/V
8.00 kHz	4.48 V	0.32 V	0.071 V/V
9.00 kHz	4.48 V	0.26 V	0.058 V/V
10.00 kHz	4.48 V	0.20 V	0.045 V/V
15.00 kHz	4.48 V	0.09 V	0.020 V/V
20.00 kHz	4.48 V	0.05 V	0.011 V/V



Conclusion: The result is good and reasonable according to the equation $\left|\frac{v_{out}}{v_{in}}\right| = \frac{\frac{\omega}{\omega_o Q}}{\sqrt{\left[1-\left(\frac{\omega}{\omega_0}\right)^2\right]^2+\left(\frac{\omega}{\omega_o}\right)^2 Q^{-2}}}$. When $f = f_o$, that is $\omega = \omega_o$, we will have $\left|\frac{v_{out}}{v_{in}}\right| = 1$ for expectation. And we can see from result that that is exactly a match.

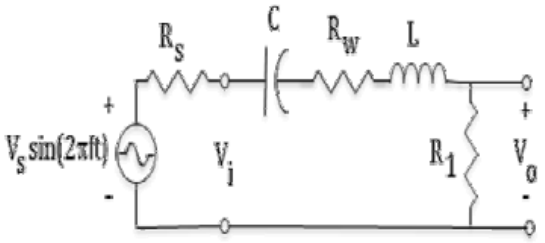
There is a little peak over 1 as seen in the graph, again, from the equation we can derive that if ω decreases with respect of ω_o, the overall denominator would decrease and thus the gain would be increased.

By looking at the graph plotting both results in step 1 and step 4, it is obvious to find that the RLC-based low pass filter is closer to the ideal case than RC circuit

because it has a faster decreasing rate for high frequencies over the resonant frequency.

5. Investigate the square waves of various frequencies with the circuit in step 4.
The procedure is similar to that in step 4. For the function generator, this time we need to change the sine wave to square wave. With a low input frequency, the output looks similar to the input. As the frequency increases, the output of the signal gradually changes its waveform to a sine wave, starting from around 1kHz.

6. Design and construct a RLC circuit to implement a band pass filter with $f_o = 5kHz$ and $Q = 5$. Also the $10mH$ inductor should be used. The circuit is shown below:



Calculation: We know that $\begin{cases} f_o = \frac{1}{2\pi\sqrt{LC}} \\ Q = \frac{2\pi f_o L}{R_w + R_1} \end{cases}$ and so we have $\begin{cases} 0.2 \times 10^{-3} s = 2\pi\sqrt{0.1 \times C} \\ 5(300 + R_1) = 2\pi \times 5000 \times 0.1 \end{cases}$.

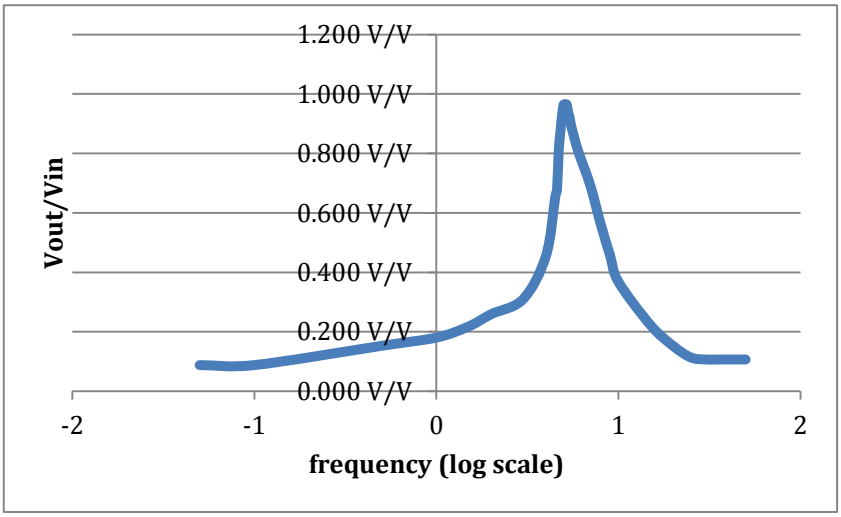
Then we can get $\begin{cases} C \approx 0.01\mu F \\ R_1 \approx 328.32\Omega \cong 330\Omega = 220\Omega + 100\Omega + 10\Omega \end{cases}$.

The measured result is shown below:

f	V_{in}	V_{out}	V_{out}/V_{in}
0.05 kHz	4.32 V	0.38 V	0.088 V/V
0.10 kHz	4.32 V	0.38 V	0.088 V/V
0.50 kHz	4.32 V	0.66 V	0.153 V/V
1.00 kHz	4.32 V	0.78 V	0.181 V/V
1.50 kHz	4.32 V	0.94 V	0.218 V/V
2.00 kHz	4.32 V	1.12 V	0.259 V/V
3.00 kHz	4.32 V	1.34 V	0.310 V/V
4.00 kHz	4.48 V	2.04 V	0.455 V/V
4.50 kHz	4.40 V	2.88 V	0.655 V/V
4.60 kHz	4.48 V	3.04 V	0.679 V/V
4.70 kHz	4.40 V	3.56 V	0.809 V/V
4.80 kHz	4.40 V	3.84 V	0.873 V/V
4.90 kHz	4.48 V	4.16 V	0.929 V/V
5.00 kHz	4.48 V	4.32 V	0.964 V/V
5.10 kHz	4.48 V	4.32 V	0.964 V/V
5.20 kHz	4.48 V	4.32 V	0.964 V/V
5.30 kHz	4.48 V	4.20 V	0.938 V/V
5.40 kHz	4.48 V	4.12 V	0.920 V/V
5.50 kHz	4.48 V	4.00 V	0.893 V/V

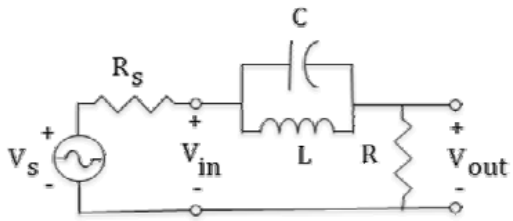
6.00 kHz	4.40 V	3.56 V	0.809 V/V
7.00 kHz	4.40 V	3.05 V	0.693 V/V
8.00 kHz	4.40 V	2.47 V	0.561 V/V
9.00 kHz	4.40 V	2.01 V	0.457 V/V
10.00 kHz	4.40 V	1.62 V	0.368 V/V
15.00 kHz	4.40 V	0.98 V	0.223 V/V
20.00 kHz	4.40 V	0.67 V	0.152 V/V
25.00 kHz	4.40 V	0.50 V	0.114 V/V
30.00 kHz	4.40 V	0.47 V	0.107 V/V
35.00 kHz	4.40 V	0.47 V	0.107 V/V
40.00 kHz	4.40 V	0.47 V	0.107 V/V
45.00 kHz	4.40 V	0.47 V	0.107 V/V
50.00 kHz	4.40 V	0.47 V	0.107 V/V

And the graph is shown below:



Conclusion: The design is presented as a band pass filter as what we expected.

7. Design and construct a circuit to implement a band reject filter with $f_o = 5kHz$ and $Q = 5$. The circuit is shown below:



Calculation: For the circuit, $\begin{cases} f_o = \frac{1}{2\pi\sqrt{LC}} \\ Q = \frac{2\pi f_o L}{R} \end{cases}$. And thus we have $\begin{cases} 0.2 \times 10^{-3} s = 2\pi\sqrt{0.1 \times C} \\ 5R = 2\pi \times 5000 \times 0.1 \end{cases}$

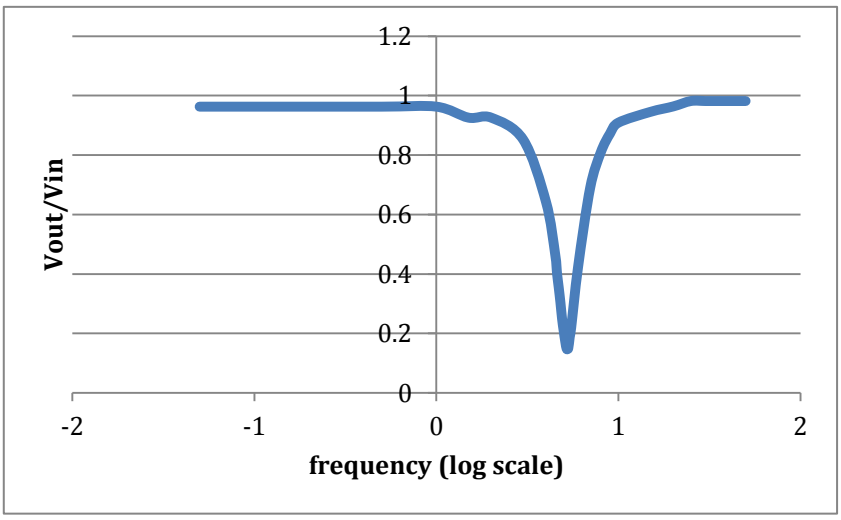
As a result, the solution is obviously: $\begin{cases} C \approx 0.01\mu F \\ R \approx 628.32\Omega \end{cases}$.

The measured result is shown below:

f	V_{in}	V_{out}	V_{out}/V_{in}

0.05 kHz	4.32 V	4.16 V	0.963 V/V
0.10 kHz	4.32 V	4.16 V	0.963 V/V
0.50 kHz	4.32 V	4.16 V	0.963 V/V
1.00 kHz	4.32 V	4.16 V	0.963 V/V
1.50 kHz	4.32 V	4.00 V	0.926 V/V
2.00 kHz	4.32 V	4.00 V	0.926 V/V
3.00 kHz	4.32 V	3.68 V	0.852 V/V
4.00 kHz	4.48 V	2.88 V	0.643 V/V
4.50 kHz	4.40 V	2.04 V	0.464 V/V
4.60 kHz	4.48 V	1.80 V	0.402 V/V
4.70 kHz	4.40 V	1.56 V	0.355 V/V
4.80 kHz	4.40 V	1.34 V	0.305 V/V
4.90 kHz	4.48 V	1.12 V	0.250 V/V
5.00 kHz	4.48 V	0.94 V	0.210 V/V
5.10 kHz	4.48 V	0.78 V	0.174 V/V
5.20 kHz	4.48 V	0.66 V	0.147 V/V
5.30 kHz	4.48 V	0.67 V	0.150 V/V
5.40 kHz	4.48 V	0.84 V	0.188 V/V
5.50 kHz	4.48 V	0.98 V	0.219 V/V
6.00 kHz	4.40 V	1.86 V	0.423 V/V
7.00 kHz	4.40 V	3.04 V	0.691 V/V
8.00 kHz	4.40 V	3.56 V	0.809 V/V
9.00 kHz	4.40 V	3.84 V	0.873 V/V
10.00 kHz	4.40 V	4.00 V	0.909 V/V
15.00 kHz	4.40 V	4.16 V	0.945 V/V
20.00 kHz	4.40 V	4.24 V	0.964 V/V
25.00 kHz	4.40 V	4.32 V	0.982 V/V
30.00 kHz	4.40 V	4.32 V	0.982 V/V
35.00 kHz	4.40 V	4.32 V	0.982 V/V
40.00 kHz	4.40 V	4.32 V	0.982 V/V
45.00 kHz	4.40 V	4.32 V	0.982 V/V
50.00 kHz	4.40 V	4.32 V	0.982 V/V

And the graph is shown below:

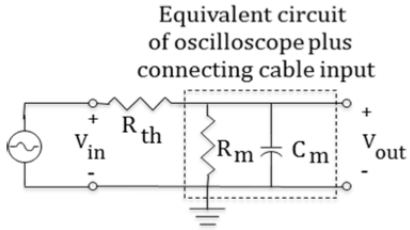


Conclusion: The design is presented as a band pass filter as what we expected.

09/25/12

Experiment #2 Parasitic Capacitance and High Frequency Measurement Problems

1. Drive the circuit shown below with a $2\,V$ peak-to-peak $20kHz$ square wave, using a coax cable with a banana plug adapter. R_{th} should be $100k\Omega$. V_{in} is connected to Cannel 1 and V_{out} is connected to Channel 2 of the oscilloscope. Compare the rising time between Ch. 1 and Ch.2, and also find the capacitance C_m.

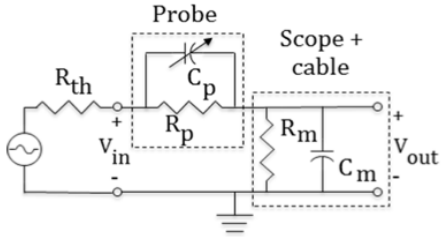


Calculation: We have the rising time of the output $t_r \approx 2.2\tau$ and $\tau = R_{in}C_{in} = R_{in}C_m$.
Assume R_m for the oscilloscope is $1M\Omega$. Then $R_{in} = R_{th} \parallel R_m \approx 90.91k\Omega$.
Thus $C_m = \frac{t_r}{2.2 \cdot R_{in}} = \frac{t_r}{200k}$.

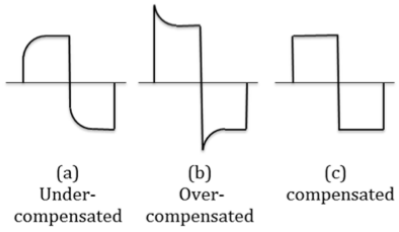
The measurement for the rising time t_r for output (Ch.2) is about $17.4\mu s$, and the rising time for input (Ch.1) is about $85ns$, which is much smaller than that of the output. Also, we can calculate C_m by the equation in the calculation section above. From the equation, we have $C_m \approx 87pF$.

Conclusion: We can see that the shunt capacitance C_m is very large when we use the banana-shaped probe. We can use a conventional X10 voltage probe to reduce it.

2. Obtain a X10 voltage probe and construct the compensated attenuator circuit shown below. Adjust C_p until we see compensation (square wave) by asserting and turning a stick into the side of the probe. Then repeat step 1 with the X10 voltage probe.



We need to connect the probe with one end to the probe composition port and another end to ground, and, of course, the channel end to either Channel 1 or 2 to see if it's compensated. C_p is adjusted until we see the square wave like part (c) in the graph below.

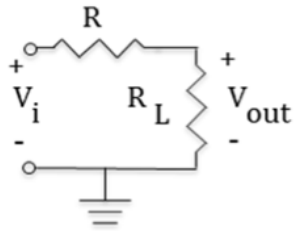


Once the probe is compensated, follow the procedure in step 1 and it is found that $t_r \approx 3.1\mu s$,

and the rising time for the input is still around $85ns$. And from the equation in step 1, we can get that $C_{m_{X10}} \approx 15.5pF$.

Conclusion: We can see that the shunt capacitance $C_{m_{X10}}$ of X10 voltage probe is much smaller than that of banana-shaped probe.

3. With the X10 voltage probe, measure the V_{out}/V_{in} as a function of frequency for the circuit shown below with $R \approx 500k\Omega$ and $R_L = 5k\Omega$.



Calculation: Ideally, we should have $V_{out} = \frac{R_L}{R+R_L}V_{in} = \frac{V_{in}}{100}$. Since we use the X10 voltage probe, $V_{in_{real}} = \frac{V_{in_{measured}}}{10}$. Thus our expected relation should be $V_{out} = \frac{V_{in}}{10}$.

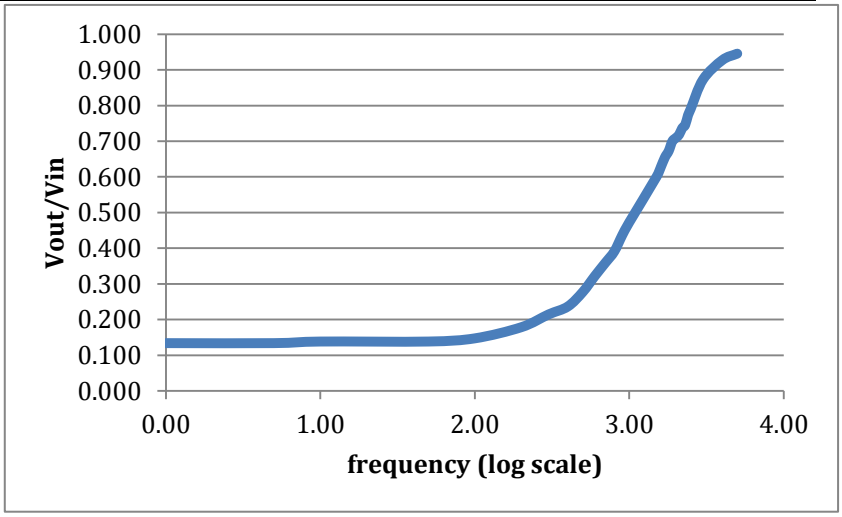
The required R is about $500k\Omega$. Since we can't find the exact value, two resistors with $1M\Omega$ in parallel are replaced with R.

And the parasitic capacitance, say C_R, can be derived from $f_{3dB} = \frac{1}{2\pi RC}$. This gives that $C_R = \frac{1}{2\pi R f_{3dB}}$.

Since we have the parasitic capacitance in shunt with the resistor R, the circuit acts like a high pass filter as the frequency changes. The measured result is shown below:

f	V_{in}	V_{out}	Adjusted Value for V_{out}/V_{in}
1.00 kHz	4.48 V	0.006 V	0.134
5.00 kHz	4.48 V	0.006 V	0.134
10.00 kHz	4.48 V	0.006 V	0.138
50.00 kHz	4.48 V	0.006 V	0.138
100.00 kHz	4.48 V	0.007 V	0.147
200.00 kHz	4.48 V	0.008 V	0.179
300.00 kHz	4.48 V	0.010 V	0.214
400.00 kHz	4.48 V	0.011 V	0.237
500.00 kHz	4.40 V	0.012 V	0.277
600.00 kHz	4.40 V	0.014 V	0.323
700.00 kHz	4.40 V	0.016 V	0.359
800.00 kHz	4.40 V	0.017 V	0.391
900.00 kHz	4.40 V	0.019 V	0.436
1000.00 kHz	4.40 V	0.021 V	0.473
1500.00 kHz	4.40 V	0.026 V	0.600
1600.00 kHz	4.40 V	0.028 V	0.627

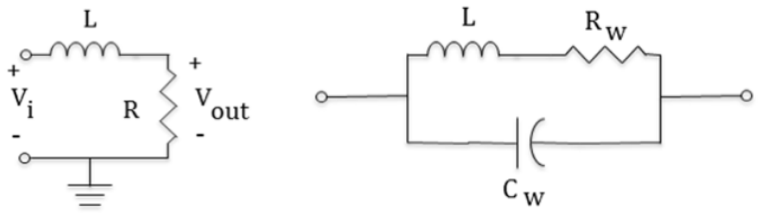
1700.00 kHz	4.40 V	0.029 V	0.655
1800.00 kHz	4.40 V	0.030 V	0.673
1900.00 kHz	4.40 V	0.031 V	0.700
2000.00 kHz	4.40 V	0.031 V	0.709
2100.00 kHz	4.40 V	0.032 V	0.718
2200.00 kHz	4.40 V	0.032 V	0.736
2300.00 kHz	4.40 V	0.033 V	0.745
2400.00 kHz	4.40 V	0.034 V	0.773
2500.00 kHz	4.40 V	0.035 V	0.791
3000.00 kHz	4.40 V	0.038 V	0.873
4000.00 kHz	4.40 V	0.041 V	0.927
5000.00 kHz	4.40 V	0.042 V	0.945



And thus the $C_R = \frac{1}{2\pi R f_{3dB}} = \frac{1}{2\pi \times 2\times 10^6 \times 5\times 10^3} = 15.9pF.$

Conclusion: This result is under expectation. As we can see from the graph, the large resistance behaves as a capacitor: with low frequency, it acts as open; and with high frequency, it acts as shorted.

4. Construct the circuit shown below (left) to estimate the L, R_w, and C_w of the equivalent circuit for the inductor from $100Hz$ to $1MHz$.



And the equivalent circuit of a physically realizable inductor is shown above (right).

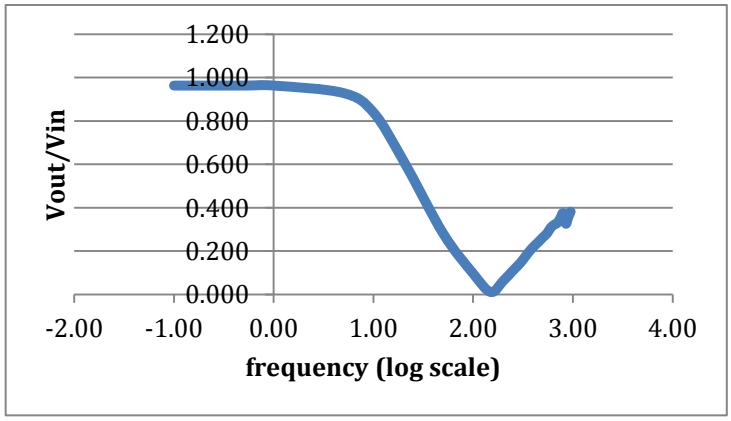
Calculation: For low frequency, C_w is open and L is short, thus we should get $\frac{V_{out}}{V_{in}} = \frac{R}{R+R_w}$.

As it reaches it's cutoff frequency, we will have the equation $f_c = (R + R_w)/2\pi L$.

Finally, when it's at the resonance frequency, the circuit becomes a RLC circuit an. The equation for the resonance frequency would be $f_o = \frac{1}{2\pi\sqrt{LC_w}}$. .

The measured results are shown below:

f	V_{in}	V_{out}	Adjusted Value for V_{out}/V_{in}
0.10 kHz	4.32 V	0.416 V	0.963 V/V
0.50 kHz	4.32 V	0.416 V	0.963 V/V
1.00 kHz	4.32 V	0.416 V	0.963 V/V
5.00 kHz	4.48 V	0.416 V	0.929 V/V
10.00 kHz	4.48 V	0.376 V	0.839 V/V
17.00 kHz	4.48 V	0.316 V	0.706 V/V
20.00 kHz	4.48 V	0.276 V	0.616 V/V
50.00 kHz	4.48 V	0.126 V	0.281 V/V
100.00 kHz	4.48 V	0.043 V	0.096 V/V
150.00 kHz	4.48 V	0.005 V	0.011 V/V
200.00 kHz	4.48 V	0.028 V	0.063 V/V
250.00 kHz	4.48 V	0.049 V	0.109 V/V
300.00 kHz	4.48 V	0.066 V	0.147 V/V
350.00 kHz	4.48 V	0.084 V	0.188 V/V
400.00 kHz	4.48 V	0.098 V	0.219 V/V
450.00 kHz	4.48 V	0.108 V	0.241 V/V
500.00 kHz	4.48 V	0.118 V	0.263 V/V
550.00 kHz	4.48 V	0.126 V	0.281 V/V
600.00 kHz	4.48 V	0.138 V	0.308 V/V
650.00 kHz	4.48 V	0.144 V	0.321 V/V
700.00 kHz	4.48 V	0.148 V	0.330 V/V
750.00 kHz	4.48 V	0.158 V	0.353 V/V
800.00 kHz	4.48 V	0.168 V	0.375 V/V
850.00 kHz	4.48 V	0.146 V	0.326 V/V
900.00 kHz	4.48 V	0.160 V	0.357 V/V
950.00 kHz	4.40 V	0.168 V	0.382 V/V
1000.00 kHz	4.40 V	0.174 V	0.395 V/V



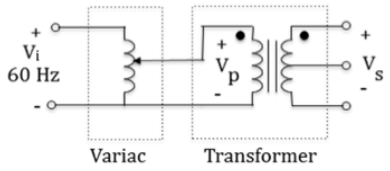
Conclusion: From the measurements, at a very low frequency like $f = 0.1kHz$, we can see that $0.963 = \frac{R}{R+R_w} \Rightarrow R_w \approx 384\Omega$. Then we can find at $f = 17kHz$, it's around the cutoff. Thus according to the equation described previously, L is derived to be $L = \frac{R+R_w}{2\pi f_c} \approx 97mH$. Finally, we can find $f = 150kHz$ is where the resonance frequency is. So we have $C_w = \frac{1}{(2\pi f_o)^2 L} \approx 11.61pF$. These values are very reasonable since we are using the $100mH$ inductor.

The graph is also under expectation. For low frequencies, C_w behaves open and L is like a short wire, then the circuit is basically a voltage divider. Thus it won't be changed in a range of low frequency inputs. As the frequency goes up, the circuit becomes RL low pass filter. When the frequency reaches a high enough point, C_w starts to influence the circuit and thus it behaves as a RLC band reject circuit.

10/07/12 & 10/14/12

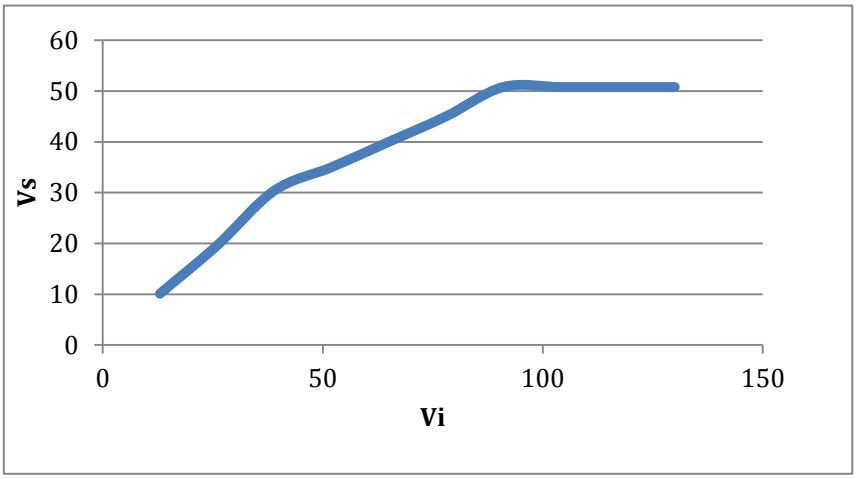
Experiment #3 Power Supplies

1. Measure the voltage across the secondary of the transformer as a function of the primary voltage. The equivalent circuit is shown below:



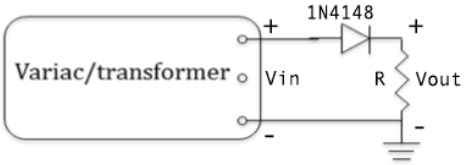
There's no calculation involves. Simply use oscilloscope to measure and record the voltages. The measurement results are shown below:

V_i/V	V_s/V
13	10.1
26	19.6
39	30.4
52	35
65	40
78	45
91	50.8
104	50.8
117	50.8
130	50.8



Conclusion: We can see as the input voltage increases, V_s increases. As V_i goes higher than $91V$, V_s stays same. It shows limitation for the transformer is no more than $50.8V$.

2. With the transformer used in step 1, connect the circuit shown below and examine the diode and resistor voltage behaviors.

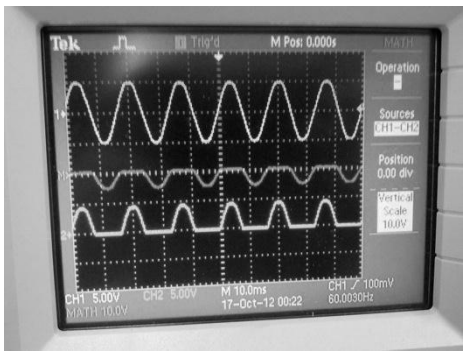


R is chosen to be $150k\Omega$, and the diode should be $1N4148$ in the lab kit.

Since the diode (1N4148) is ungrounded, it is not appropriate to use a single oscilloscope. The solution is to use two instead of one to measure the voltage across the transformer (V_{in}) and the voltage across the resistance (V_{out}). And for the voltage across the diode, $V_{diode} = V_{in} - V_{out}$.

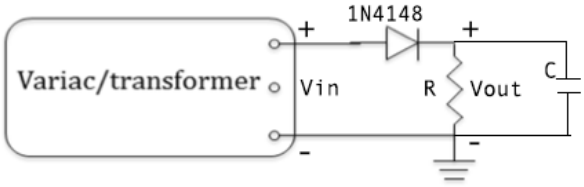
The waveforms are shown below:

V_{in}
V_{diode}
V_{out}



Conclusion: The result is reasonable. For the positive input voltage, the diode behaves as a short wire and thus no voltage across it. For the negative input voltage, the diode then changes as an open wire, and thus the voltage across it equals the input voltage, which gives V_{out} a $0V$.

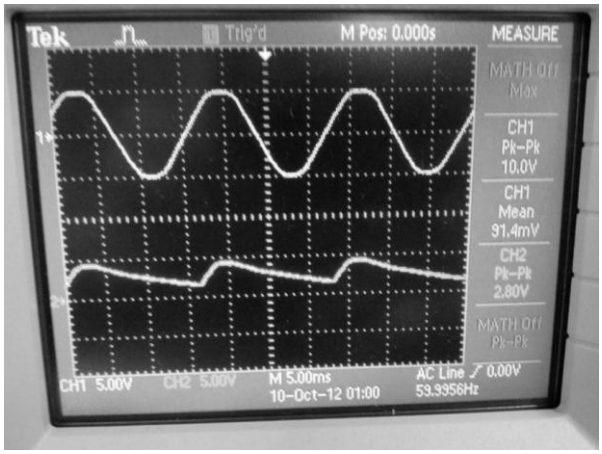
3. Place a suitable capacitor across the resistor in step 2 and observe the change of waveform. The time constant $\tau = RC$ should be about $15ms$.
The circuit is shown below:



Calculation: Since we want $\tau = RC = 15ms$, and we have $R = 150k\Omega$. Thus $C = \frac{\tau}{R} = 0.1\mu F$.

With the same measurement method, we have the waveforms:

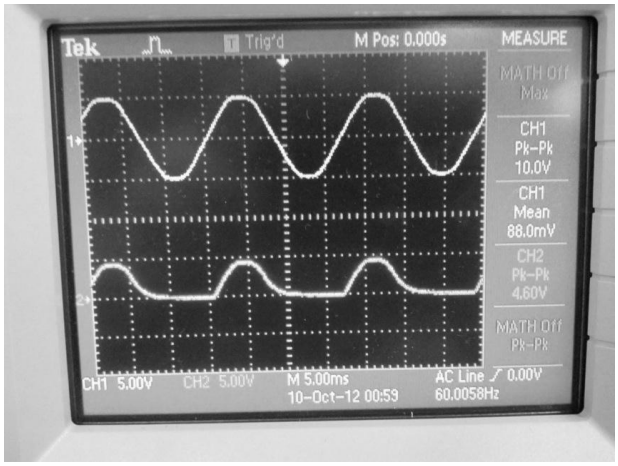
V_{in} vs V_{out}



Conclusion: Due to the time constant, the output voltage skews.

4. Repeat step 3 with a different capacitor.
The capacitor with $C = 0.01\mu F$ is chosen.
Calculation: $\tau = RC = 150k\Omega \times 0.01\mu F = 1.5ms$.

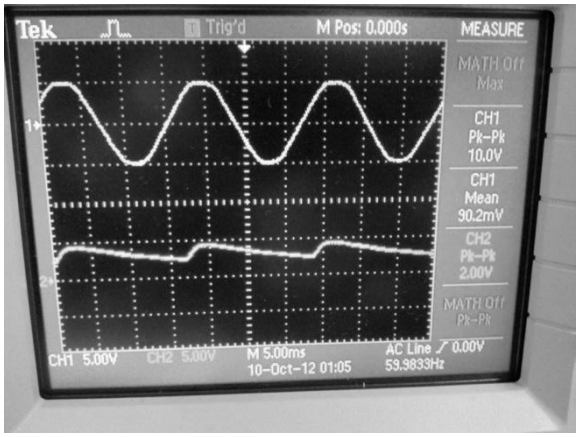
V_{in} vs V_{out}



Conclusion: Due to a smaller time constant, the output voltage skews less than that in step 3.

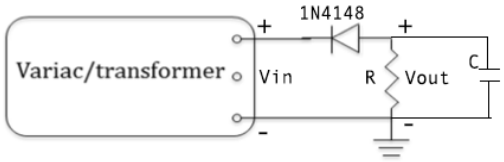
5. Repeat step 3 with a different load resistance.
The capacitor with $R = 300k\Omega$ is chosen.
Calculation: $\tau = RC = 300k\Omega \times 0.1\mu F = 30ms$.

V_{in} vs V_{out}



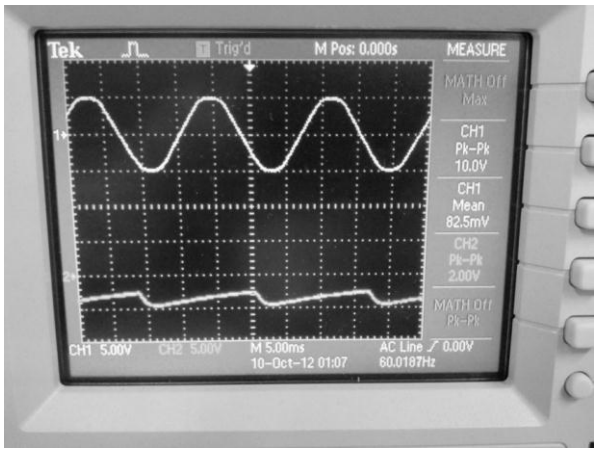
Conclusion: Due to a larger time constant, the output voltage skews more than that in step 3. Moreover, it is behaves as a DC voltage.

6. Choose one circuit from step 3, 4, and 5 which has a minimum ripple in the load voltage. Check the effect of reversing the polarities of both the diode and the capacitor.
The circuit is shown below:



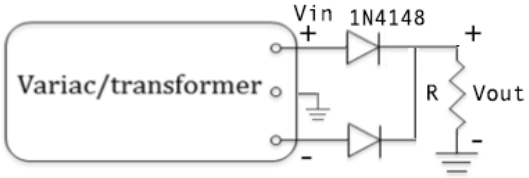
We can see that step 5 has the minimum ripple across the load voltage. Thus use the same configuration in step 5 with $C = 0.1\mu F$ and $R = 300k\Omega$. The waveform is shown below:

V_{in} vs V_{out}

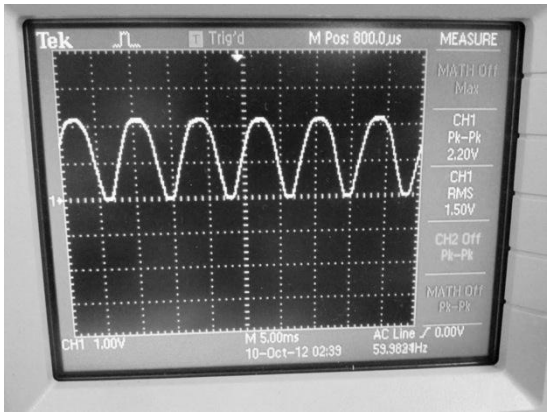


Conclusion: The result is very reasonable. When we flip the diode, positive input voltage is blocked and negative input voltage passes across the diode. Thus V_{out} is exactly a flip-over version comparing with that in step 5.

7. Design and verify a circuit that load current flows on both half-cycles of the 60Hz input (known as a "full-wave" circuit). It should contain 2 diodes and 1 resistor.
The circuit is shown below:



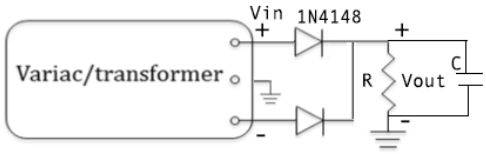
The diode is $1N4148$ and $R = 1k\Omega$. And the waveform is shown below:



Conclusion: Two diodes with one on positive side and one on negative side gives a result that both positive and negative input voltage can pass the diode. For positive input voltage, diode on the top is on and the other is off. Similarly, diode on the bottom is on and the other is on for negative input voltage.

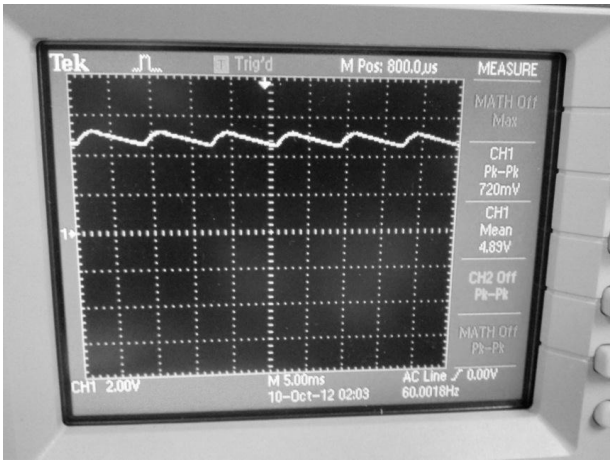
8. Modify the circuit in step 7 to make the load voltage the best possible approximation to a DC voltage.

The solution is to add a capacitor in parallel with the load resistor. The modified circuit is shown below:



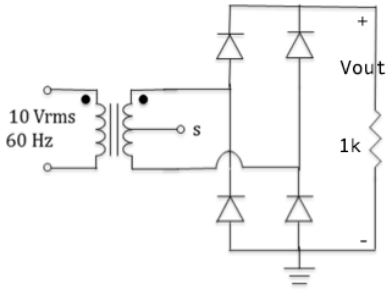
Calculation: To make the output voltage an approximation of a DC voltage, we need a relatively large RC time constant. We have $R = 1k\Omega$, then $C = 47\mu F$ is a good choice so that $\tau = RC = 47ms$.

The waveform is then shown below:



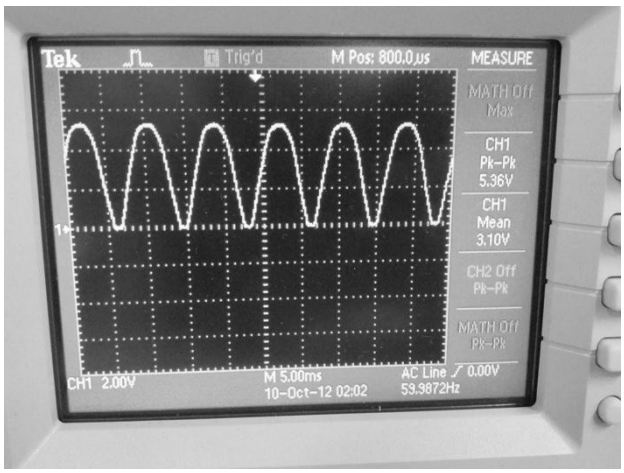
Conclusion: The waveform proves that the design is a good approximation to a DC voltage since the ripple voltage is very small. It should be clear that the larger the time constant is, the smaller the ripple voltage becomes, and the better the approximation to a DC voltage is. Vice versa.

9. Investigate the following power supply circuit below.



Built this bridge circuit with the $1N4148$ diodes and the $1k\Omega$ resistor.

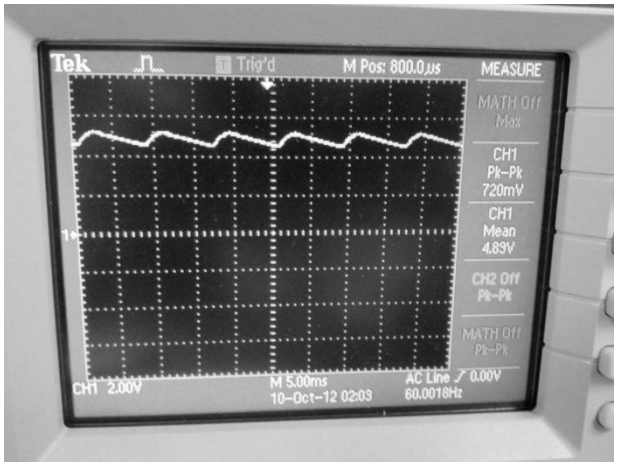
Measure the output voltage and then the waveform is derived and shown below:



Conclusion: Unlike the full-wave circuit in step 7, the use of four diodes in the bridge circuit behaves more accurate. The waveform itself is very similar to that in step 7.

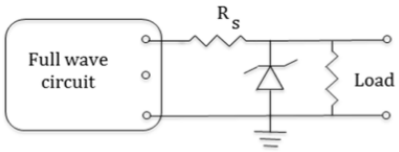
10. Add capacitive filtering to the circuit in step 9.

Basically it is a similar question in step 8. If a capacitor with $C = 47\mu F$ is asserted in parallel with the resistor, we will again have a time constant of $47ms$ as we calculated before in step 7. And the waveform is shown below:



Conclusion: The large time constant results in a good approximation to DC voltage for the output. The result is very reasonable and similar to what we get in step 8.

11. Add a Zener regulator to the output of the full-wave rectifier. Design the regulator so that the load current may be varied from 0 to $20mA$ while the load voltage varies by no more than 1%. The circuit is shown below:



The Zener diode is a type of $1N4740$.

Calculation: We have $V_{in} = 15V$ and $0 < I_{load} < 20mA$. From the datasheet of the Zener diode has a characteristic of $V_z = 10V$ and $I_z = 25mA$.

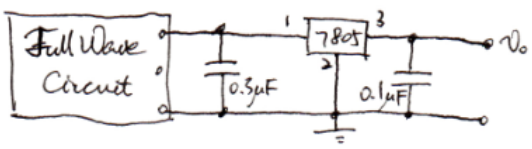
Thus $(I_{load} + I_z)R_s + V_z = V_{in}$ gives $R_s = \frac{V_{in} - V_Z}{I_{load} + I_z} = \frac{15V - 10V}{20mA + 25mA} \approx 100\Omega$.

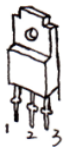
The measurement results are shown below:

R_L $(k\Omega)$	V_L (V)	V_L/R_L (mA)
∞	10	0
2	9.4	4.7
1	9	9
0.5	8.2	16.4

Conclusion: The design is good. As R_L varies, the results do not exceed the range from 0 to $20mA$.

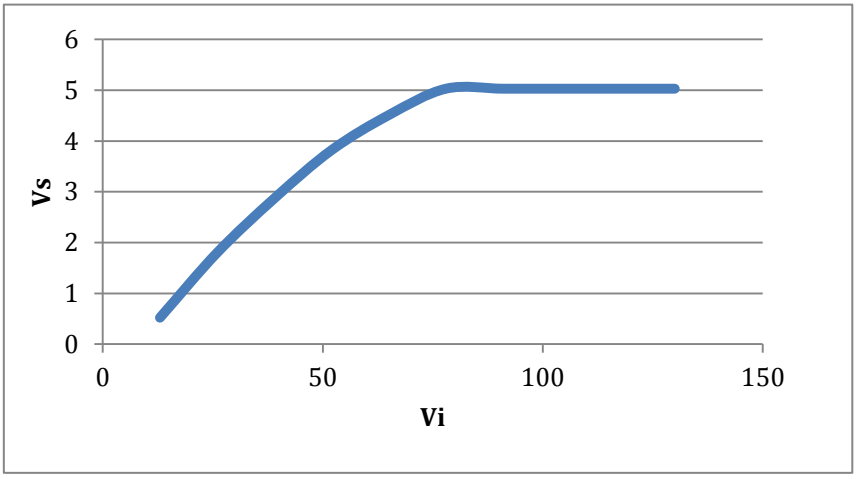
12. Measure the output voltage of the 7805 voltage regulator over appropriate ranges of input voltage and load current. The circuit is shown below:



and 

And the measurement results are shown below:

V_i/V	V_s/V
13	0.52
26	1.80
39	2.87
52	3.82
65	4.51
78	5.03
91	5.03
104	5.03
117	5.03
130	5.03



Conclusion: As the graph shows, V_s increases as V_i increases. Once V_i goes beyond $78V$, V_s remains to be $5.03V$. Therefore, the limitation for the regulator is about $5.03V$.

10/21/12

Experiment #4 Differential Amplifiers

I. Abstract

This lab revolves around the design and behaviors of differential amplifiers. Designs are performed to meet the required specifications, and measurements on currents and voltages are taken to verify the amplifiers. To further understand the behaviors of differential amplifiers, a current source is designed and constructed to replace the emitter resistor and keeps the functionality of the amplifier designed before. The verification is a determination of the base-emitter voltage, the single-ended common mode gain, single-ended differential mode gain, and the common mode rejection ratio (CMRR).

II. Introduction

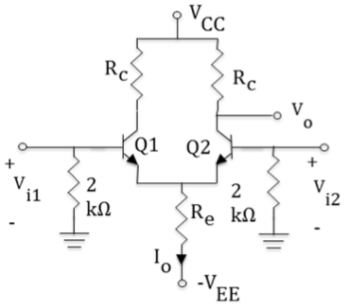
This experiment is separated into two main parts: the design of an amplifier with the emitter resistor asserted, and another design of the current source replacement. Each part is divided into three sections, which are the design process, the measurements for common mode gain and differential mode gain, and the estimation of CMRR.

Before the lab starts, some knowledge should be clearly understood. The BJT transistors should be active for the experiments, which means that $V_{BE} \geq 0.7V$ and $0.4V < V_{CB}$. Moreover, common mode gain is $A_{cm} \equiv \frac{V_o}{V_{cm}}$, differential mode gain is $A_d \equiv \frac{V_o}{V_d}$, and $CMRR = 20 \log \left|\frac{A_d}{A_{cm}}\right|$. In the experiments, it is assumed that the transistors in used have same specifications, that is, g_m is same for all transistors.

III. Experiment

Part 1 - Differential Amplifier with the emitter resistor R_e asserted.

1. *Design and verify the differential amplifier shown on the right side so that $I_o < 10mA$, $R_e < 2k\Omega$, and $v_{c1} = v_{c2} = v_o > 10V$ peak-to-peak for the differential input signal. We have $V_{CC} = -V_{EE} = 15V$.*



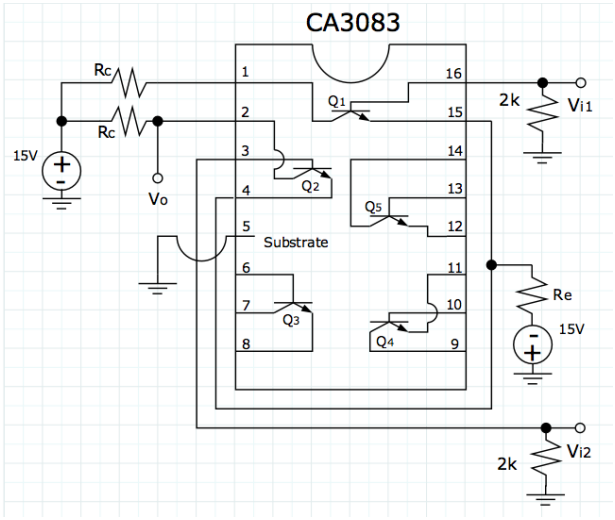
To make sure the BJT transistors are in active mode, $V_{BE} = 0.7V$ is required. Since it is assumed that g_m is same for all transistors, $R_e = \frac{0 - V_{BE} - (-V_{EE})}{I_o} = \frac{14.3V}{I_o}$. For $R_e < 2k\Omega$, $I_o > 7.15mA$. For $I_o < 10mA$, $R_e > 1.43k\Omega$. Thus, $1.43k\Omega < R_e < 2k\Omega$, and $7.15mA < I_o < 10mA$.

Therefore, it is reasonable to choose $R_e = 1.5k\Omega$, and then the expected $I_o = \frac{14.3V}{R_e} \approx 9.53mA$. Since it is hard to find a $1.5k\Omega$ resistor, one $1k\Omega$ resistor is in series with the parallel of two $1k\Omega$ resistors so that $R_e = 1k\Omega + (1k\Omega \parallel 1k\Omega) = 1.5k\Omega$.

Now suppose $v_o > 10V$ for AC signals. Since the maximum allowable range for V_{CB} is between $0.4V$ and $15V$, we must have $5.4V < V_{CE} < 10V$ due to the AC signal swing, and thus $4.7V < V_o < 9.3V$. Then $R_C = \frac{V_{CC} - V_o}{I_o/2}$ gives $1.18k\Omega <$

$R_C < 2.16k\Omega$. Choose $R_C = 2k\Omega$.

The circuit is constructed as shown below:



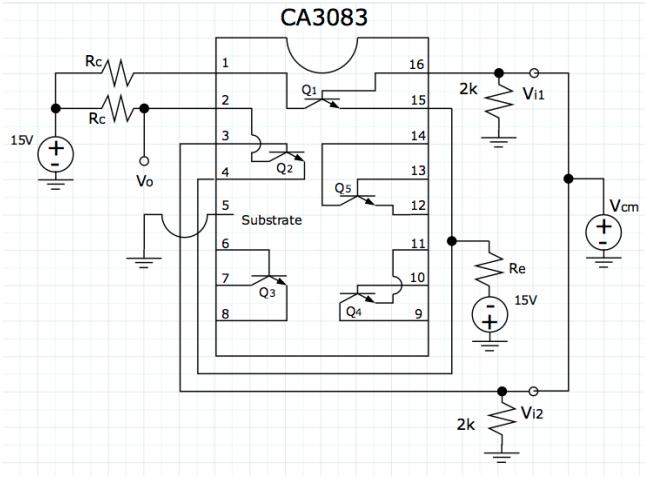
To verify the amplifier, V_{i1} and V_{i2} are connected to ground and a multi-meter is used to test the voltages across V_{BE1} (pin 16 and 15) and V_{BE2} (pin 3 and 4) and the current I_o (across R_e).

2. *Measure the single-ended common mode gain at* $1kHz$.

To do this, V_o (peak-to-peak) is measured via the oscilloscope while an input signal is provided by the function generator so that $V_{i1} = V_{i2} = V_{cm}$.

Assume $I_o = 9.53mA$. Then it is expected that $g_m = \frac{I_C}{V_T} = \frac{I_o}{2V_T} \approx 0.19A/V$ and $|A_{cms}| \approx \frac{g_m R_C}{1+g_m R_C \frac{2R_e}{R_C}}$ assuming $r_o \gg R_C$. This gives $|A_{cm}|$ should be around $0.665V/V$.

The circuit construction is shown below:

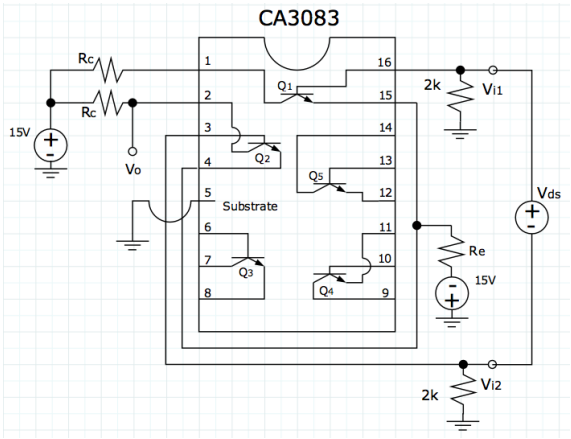


3. *Measure the single-ended differential mode gain at* $1kHz$. *Use the result to estimate CMRR.*

Similarly, V_o (peak-to-peak) is measured via the oscilloscope. This time, $V_{i1} = -V_{i2} = \frac{V_{ds}}{2}$, and thus $|A_{ds}| = \frac{V_o}{V_{ds}}$. The expected $|A_{ds}| \approx \frac{g_m R_C}{2}$ assuming

$r_o \gg R_C$, and this gives $|A_{ds}|$ should be around $190V/V$. Therefore, $CMRR = 20\log\left|\frac{A_{ds}}{A_{cms}}\right| \approx 49.12dB$.

The circuit construction is shown below:

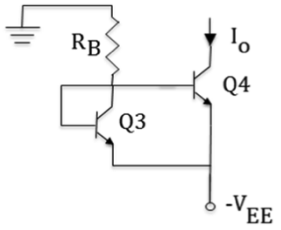


4. *Use differential input signals to measure the output signal swing capability before clipping occurs.*

This is basically a question about the maximum input voltage V_{ds} that keeps the output waveform stays as a sinusoidal wave. It is done by varying the input voltage V_{ds} in the circuit constructed in step 3, and the output signal should be observed when it starts to clip.

Part 2 - Differential Amplifier with the current source asserted.

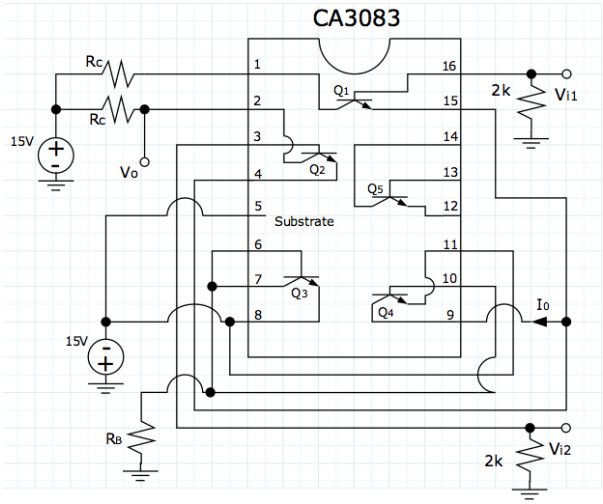
1. *Replace the emitter resistor R_e with the current source shown on the right side. Design and verify the current source so that the current I_o remains the same in part 1.*



Due to the measured value $I_o = 9.63mA$ and it remains, R_B should be chosen carefully. It is clear to see that $R_B I_o = 0 - V_{BE} - (-V_{EE})$ from the graph.

Therefore, $R_B = \frac{14.3V}{9.63mA} \approx 1.5k\Omega$. Similarly, use three resistors that one $1k\Omega$ resistor is in series with the parallel of two $1k\Omega$ resistors in order to achieve $R_e = 1k\Omega + (1k\Omega \parallel 1k\Omega) = 1.5k\Omega$.

The circuit should be constructed as shown below:



To verify the amplifier, again, V_{i1} and V_{i2} are connected to ground and a multi-meter is used to test the voltages across V_{BE1} (pin 16 and 15), V_{BE2} (pin 3 and 4), V_{BE3} (pin 6 and 8), and V_{BE4} (pin 10 and 11) and the current I_o.

2. *Measure the single-ended common mode gain at* $1kHz$.

This is just a repeat of section 2 in part 1 with the differential amplifier shown above. Set $V_{i1} = V_{i2} = V_{cm} = 1.5V$ at $f = 1kHz$ for the input signal and measure the output V_o (peak-to-peak) via the oscilloscope. The expected result should be same as it is expected in part 1, which is around $0.665V/V$.

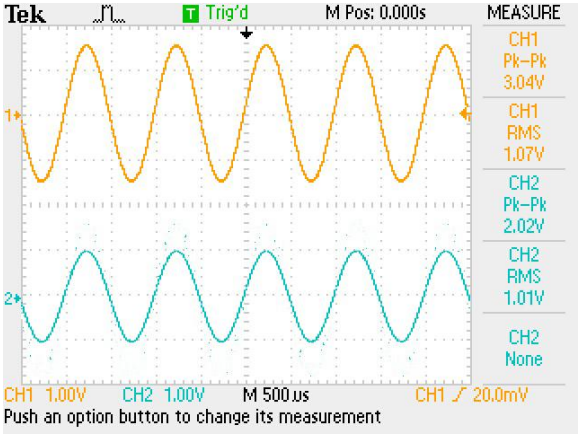
3. *Measure the single-ended differential mode gain at* $1kHz$. *Use the result to estimate CMRR.*

It is a repeat of section 3 in part 1 with a different amplifier. Set $V_{i1} = -V_{i2} = \frac{V_{ds}}{2}$ and measure the output voltage via the oscilloscope. The result should be same as it is expected in part 1, which is around $190V/V$. Hence, CMRR should remain same.

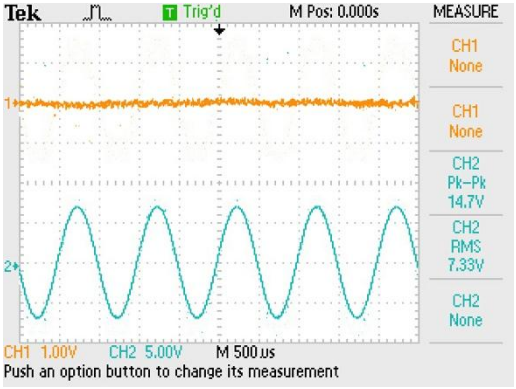
IV. Results

Part 1 - Differential Amplifier with the emitter resistor R_e asserted.

1. It is measured via the multi-meter that $V_{BE1} = 682.4mV \approx 0.7V$, $V_{BE2} = 682.9mV \approx 0.7V$, and $I_o = 9.63mA$. The result shows that the design meets the requirement. The actual measured current I_o has an error of 1% than expected value. This confirms that the designed amplifier is working.
2. Given the input $V_{cm} = V_{i1} = V_{i2} = 1.5V$ (Vpp), it is measured that $V_o = 2.02V$ (peak-to-peak) and $V_{cm} = 3.04V$ (peak-to-peak). Hence, we have $A_{cm} = \frac{2V_o}{V_{i2}+V_{i1}} = \frac{V_o}{V_{cm}} \approx 0.6645V/V$. This result is very close to the expected value with an error of 0.075%.



3. Give $V_d = 50mV$ (Vpp), it is measured that $V_o = 14.7V$. Hence, we can get that $A_d = \frac{V_o}{V_{i1}-V_{i2}} = 147V/V$. Therefore $CMRR = 20\log_{10}\left|\frac{A_d}{A_{cm}}\right| = 20\log_{10}\frac{147}{0.6645} \approx 46.9dB$.

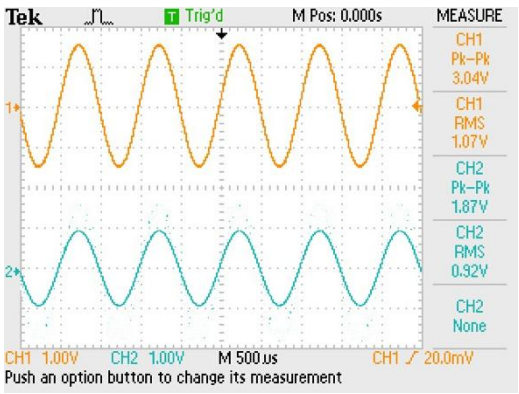


There exist a huge error for A_d (22.6%). The expected value is $A_d = 190V/V$. One of the reasons might be that r_o is not ideally much larger than R_C. Another possible explanation is that the differential current is very small and causes an "unstable" amplification.

4. As V_d reaches $56mV$ (Vpp), the output signal starts to clip. At $V_d = 56mV$ (Vpp), the output signal $V_o = 15.43V$. Thus the output signal swing capability is around $15.43V$.

Part 2 - Differential Amplifier with the current source asserted.

1. It is measured via the multi-meter that $I_o = 9.72mA$, which still meets the requirement with an error of 0.9% than previous measured current. Also $V_{BE1} = 707.1mV \approx 0.7V$ and $V_{BE2} = 707.2mV \approx 0.7V$. Thus the design is verified to be working.
2. Given the input $V_{cm} = V_{i1} = V_{i2} = 1.5V$ (Vpp), it is measured that $V_{cm} = 3.04V$ and $V_o = 1.87V$ (peak-to-peak). Hence, $A_{cm} = \frac{2V_o}{V_{i2}+V_{i1}} = \frac{V_o}{V_{cm}} = 0.615V/V$.



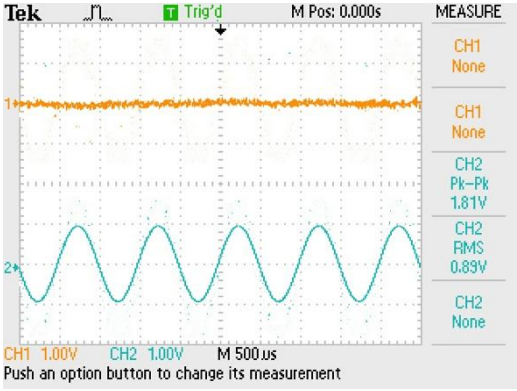
There is an error of 7.52%, which is relatively large. The reason might be that

the replaced current mirror does not behave ideally as what we expected.

3. Given $V_d = 8mV$, it is measured that $V_o = 1.81V$. Hence, we have $A_d = \frac{V_o}{V_{i1} - V_{i2}} = 226.25V/V$.

$$CMRR = 20\log_{10}\left|\frac{A_d}{A_{cm}}\right| \approx 51.31dB.$$

Again the error here is very large. One possible reason is due to the behavior of the replaced current mirror. As the expected I_o increases, with the unstable feature discovered in part 1, a significant increase of the amplified output voltage should be realized.



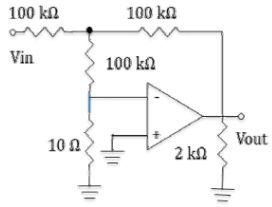
V. Conclusion

This lab focuses on the discovery of the characteristics of differential amplifiers. First four sections help students understand basic properties of the differential amplifiers that the common-mode gain is much smaller than the differential-mode gain. The differential amplifiers have a significant benefit to see the difference of an input signal. The rest of three sections help students explore the practical applicability of current mirror. In all, theoretical analysis for differential amplifiers is verified through experimental measurements.

10/30/12

Experiment #6 Operational Amplifiers

1. Determine the open loop gain A_v of the 741 op amp by measuring the input and output voltages in the circuit shown below. Also find the DC open loop gain.



Calculation: Let the voltage at the conjunction point among three $100k\Omega$ be V_1. Assume the op amp has infinite input resistance, zero output resistance and a finite voltage gain A_v. Then we must $V_{out} = -A_v V_1 \frac{10}{100k} = -A_v V_1 \times 10^{-4}$

Then Kirchhoff's law tells $\frac{V_{in}-V_1}{100k\Omega} = \frac{V_1}{100k\Omega+10\Omega} + \frac{V_1}{100k\Omega+2k\Omega}$. Since $100k\Omega$ is very large compare with $2k\Omega$ and 10Ω, it is reasonable to approximate the equation as $\frac{V_{in}-V_1}{100k\Omega} = \frac{V_1}{100k\Omega} + \frac{V_1}{100k\Omega} \Rightarrow V_{in} = 3V_1$.

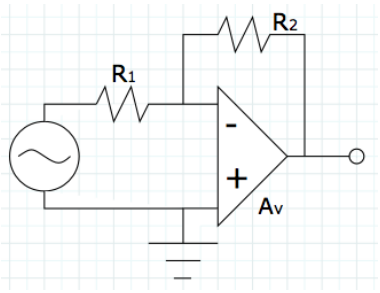
Thus, $V_{in} = -3 \times 10^4 \frac{V_{out}}{A_v} \Rightarrow A_v = -\frac{V_{out}}{V_{in}} \times 3 \times 10^4$.

Now construct the circuit with IC LM741N. Control the amplitude of the input so that the output waveform is not distorted. It is measured that at that moment $V_{in} = 5.4V$ at $1Hz$ and $V_{out} = 0.96V$.

Conclusion: From the measurement, we can find that $A_v = -\frac{0.96}{5.4} \times 3 \times 10^4 \approx 5333V/V$.

2. Construct an inverting amplifier with a voltage gain of 5 and investigate the linearity and dynamic range of its output as a function of op amp supply voltages for an input sinusoidal signal at $1kHz$.

The circuit is shown below.

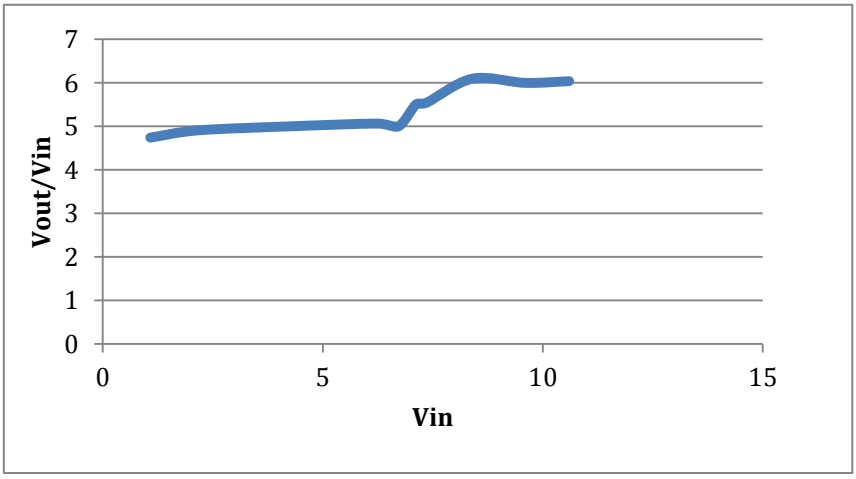


Calculation: We need $A_v = \frac{V_{out}}{V_{in}} = -5$ and $\frac{V_{in}}{R_1} = -\frac{V_{out}}{R_2}$. Thus $\frac{R_2}{R_1} = 5$.

We choose $R_1 = 2k\Omega$ and $R_2 = 10k\Omega$.

The measured results are shown below:

V_{in}/V	V_{out}/V
1.08	5.12
2.16	10.6
4.24	21.2
6.24	31.6
6.72	33.6
7.12	39.2
7.36	40.8
8.4	51.2
9.6	57.6
10.6	64



Conclusion: As it is seen in the graph above, we can find the voltage gain remains around 5 until the input voltage reaches $7.12V$. Thus, it is a reasonable approximation that the linearity range of the output would be from $0V$ to $7V$. Also the dynamic range would be approximately greater than $7V$.

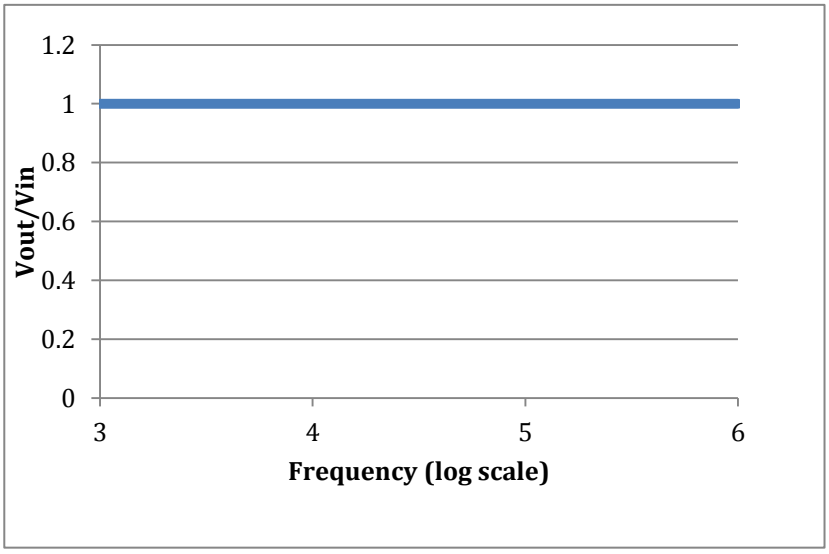
3. Measure the voltage gain versus frequency for an amplifier that has gains of 1, 5, 20, and 40.

Calculation: $|A_v| = 1$ or 5 or 20 or 40 gives $R_2 = 1k\Omega$ or $5k\Omega$ or $20k\Omega$ or $40k\Omega$ respectively if we fix $R_1 = 1k\Omega$.

Circuit construction is same as in part 2. The input voltage is fixed to be $2.16V$ as it is measured.

For $|A_v| = 1$, $R_1 = 1k\Omega = R_2$, the result is shown below:

Frequency *(kHz)*	V_{out} *(V)*
1	2.16
10	2.16
100	2.16
300	2.16
350	2.16
400	2.16
450	2.16
500	2.16
550	2.16
600	2.16
700	2.16
800	2.16
900	2.16
1000	2.16

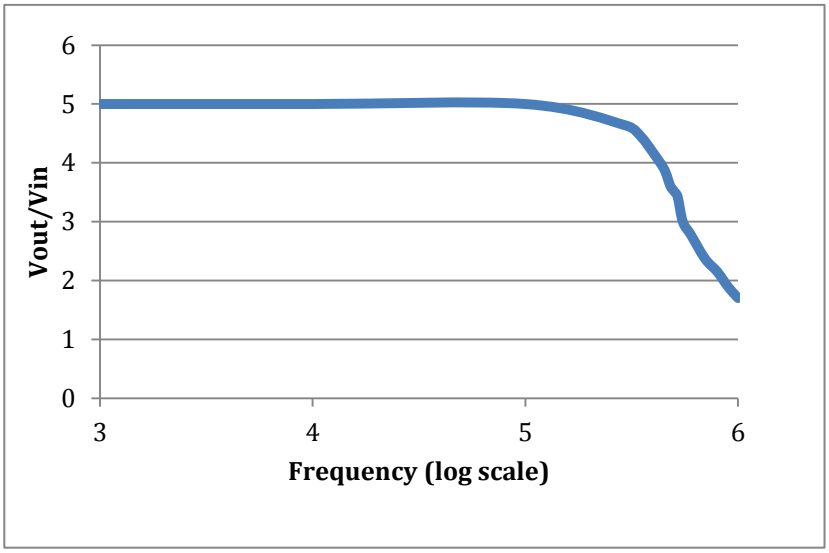


f_{3dB} can't be found since the maximum frequency output is $1MHz$

Thus f_{3dB} must be greater than $1MHz$

For $|A_v| = 5$, $R_1 = 1k\Omega$ and $R_2 = 5k\Omega$, the result is shown below:

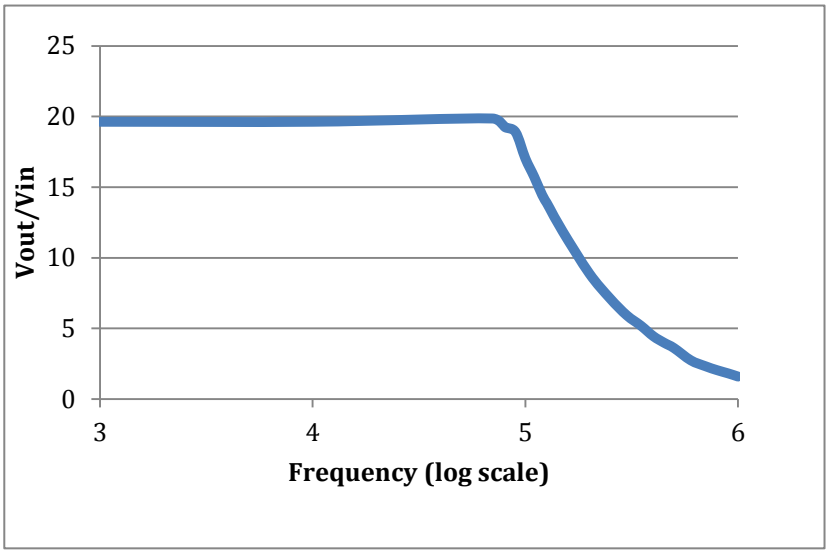
Frequency *(kHz)*	V_{out} *(V)*
1	10.8
10	10.8
100	10.8
300	10
350	9.6
400	9
450	8.4
480	7.8
500	7.6
520	7.4
550	6.48
600	6
700	5.12
800	4.64
900	4.08
1000	3.68



$f_{3dB} = 500kHz$

For $|A_v| = 20$, $R_1 = 1k\Omega$ and $R_2 = 20k\Omega$, the result is shown below:

Frequency *(kHz)*	V_{out} *(V)*
1	42.4
10	42.4
70	42.9
80	41.6
90	40.8
100	36.8
110	34
120	31.2
126	30
130	29.2
150	25.6
200	19.2
250	15.4
300	12.8
350	11.2
400	9.6
450	8.6
500	7.8
600	5.92
700	5.04

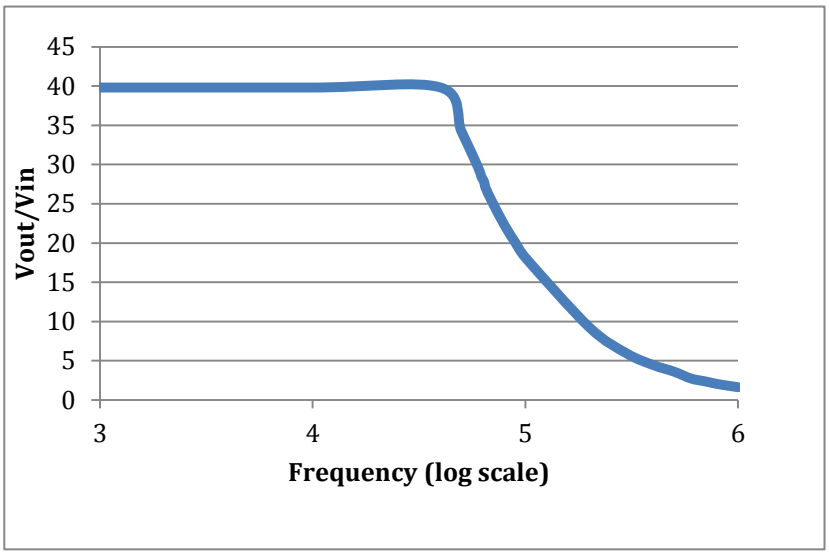


$f_{3dB} = 126kHz$

800	4.40
900	3.92
1000	3.44

For $|A_v| = 40$, $R_1 = 1k\Omega$ and $R_2 = 40k\Omega$, the result is shown below:

Frequency *(kHz)*	V_{out} *(V)*
1	86
10	86
40	86
50	74
60	64
62	61.6
63	60.8
64	60
65	58.4
70	54.4
80	48
90	43.2
100	39.2
200	20
300	12.8
400	9.6
500	7.8
600	5.92
700	5.12
800	4.40
900	3.92
1000	3.52

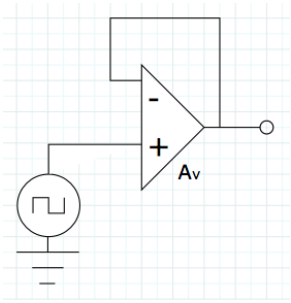


$f_{3dB} = 63kHz$

Conclusion: As we can see from all the results shown above, the cutoff frequency f_{3dB} is decreasing as the open loop gain $|A_v|$ increasing. Therefore, to deduce the open loop pole frequency of the op amp, we can simply increase the open loop gain $|A_v|$. That is, increase the ratio of $\frac{R_2}{R_1}$, and we want a smaller R_1 and a larger R_2.

4. Determine the slew rate of the op amp using a unity-gain voltage follower with a square wave input signal $v_s(t)$ at $50kHz$. Also investigate with a sinusoidal wave.

The circuit is shown on the right side.



To investigate with the sinusoidal wave, just change the function generator to be "sinusoidal wave" instead of "square wave".

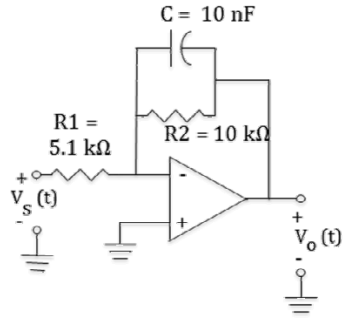
Calculation: Theoretically, the slew rate should be $2\pi fV$, where f is the signal frequency and V is the maximum undistorted output amplitude.

To calculate the slew rate with actual measured results, we can use the equation $\frac{\Delta V}{\Delta t} = \frac{90\%V - 10\%V}{T_1 - T_2} = \frac{0.8V}{rising\ time}$.

The measured results for square wave are $V_{in} = 2.24V$ and $t_{rising} = 1.84\mu s$.

Conclusion: We then have $slew\ rate = \frac{0.8 \times 2.24V}{1.84\mu s} \approx 0.97V/\mu s$. Theoretically, it should be $2\pi \times 50kHz \times 2.24V \approx 0.7V/\mu s$. This has a large error due to the inaccurate approximation on the oscilloscope.

5. Construct the circuit below and determine its transfer characteristic and its cutoff frequency f_{3dB}.

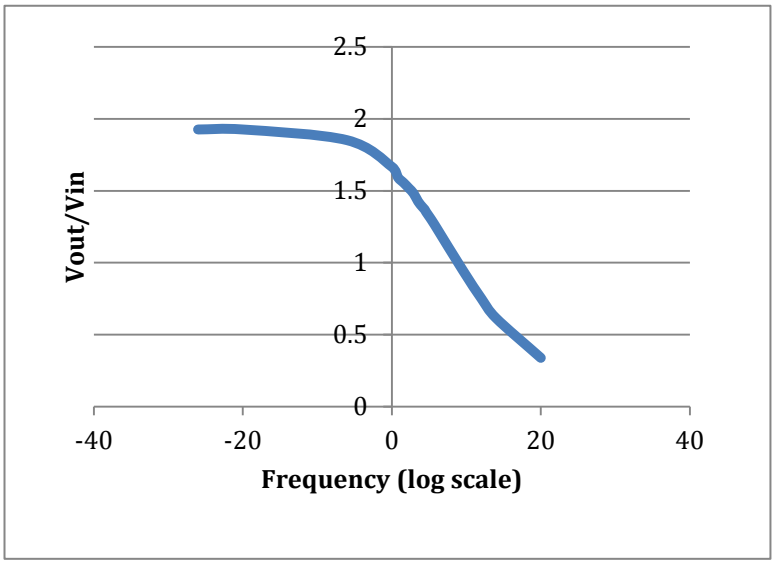


Also compare the low frequency gain and the cutoff frequency with the theoretical values.

Calculation: Theoretically, we have $|A_o| = \frac{R_2}{R_1} = 1.96$ and $\omega_{3dB} = \frac{1}{R_2 C} = 10000 rad/s$.

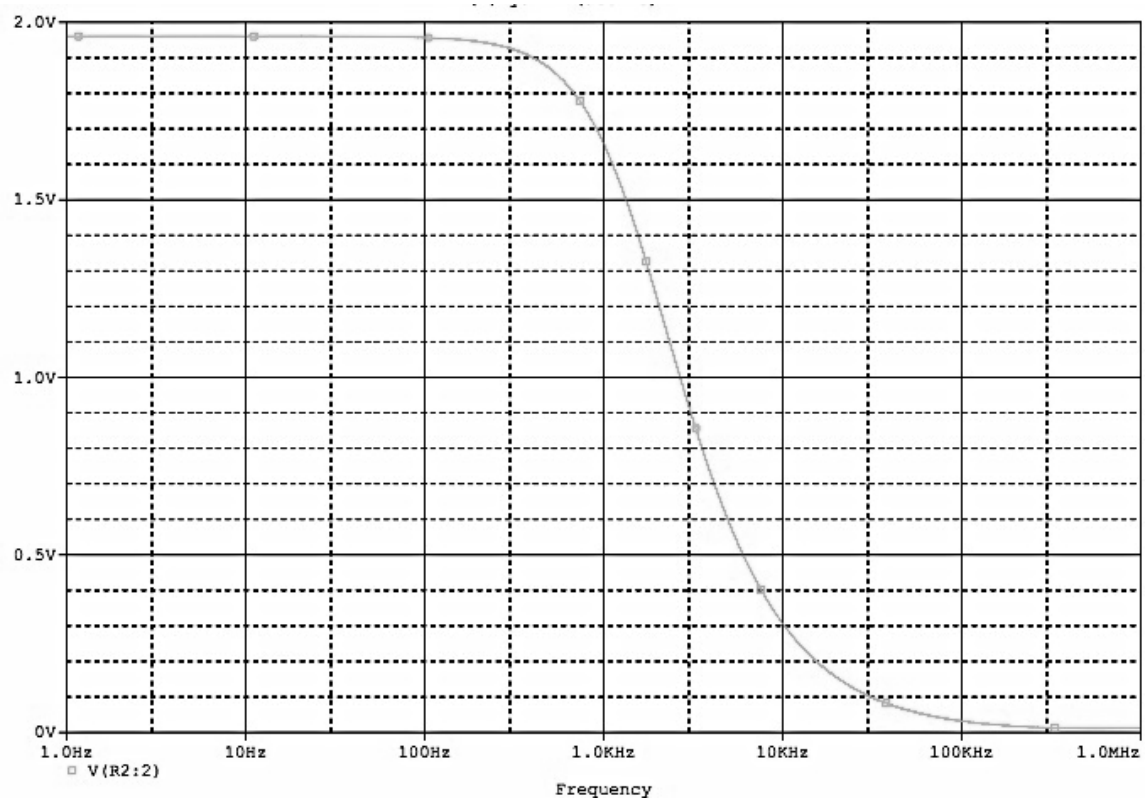
The measured results are shown below:

Frequency *(kHz)*	V_{in} *(V)*	V_{out} *(V)*
0.05	2.16	4.16
0.1	2.16	4.16
0.5	2.16	4.00
1	2.16	3.60
1.1	2.16	3.44
1.2	2.16	3.36
1.3	2.16	3.28
1.4	2.16	3.20
1.5	2.16	3.08
1.6	2.16	3.00
1.66	2.16	2.96
1.7	2.16	2.92
1.8	2.16	2.84
1.9	2.16	2.76
2	2.16	2.68
3	2.24	2.12
4	2.24	1.68
5	2.24	1.38
10	2.24	0.76



$f_{3dB} = 1.66kHz$ and $\omega_{3dB} = 2\pi f_{3dB} \approx 10430.1 rad/s$

The PSpice result is shown below:

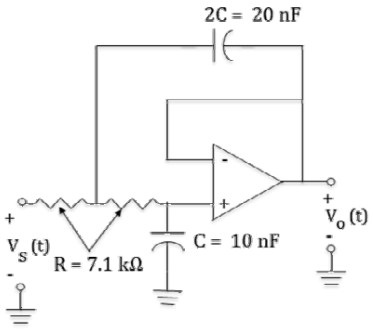


Evaluate	Measurement	Value
☒	Cutoff_Lowpass_3dB(V(U1:OUT))	1.58284k

Conclusion: At low frequency, we have $A_{o_{experimental}} = \frac{4.16}{2.16} \approx 1.93V/V$. This is very close to the expected value, $A_o = 1.96V/V$. And $\omega_{3dB_{experimental}} = 10.43krad/s$, which is also very close to our expected value $\omega_{3dB} = 10krad/s$. Therefore, our experiment proves the theoretical equations.

From the graph, it is not hard to see that this circuit implements the low-pass filter and f_{3dB} is reasonably close to the result we achieved in measurements.

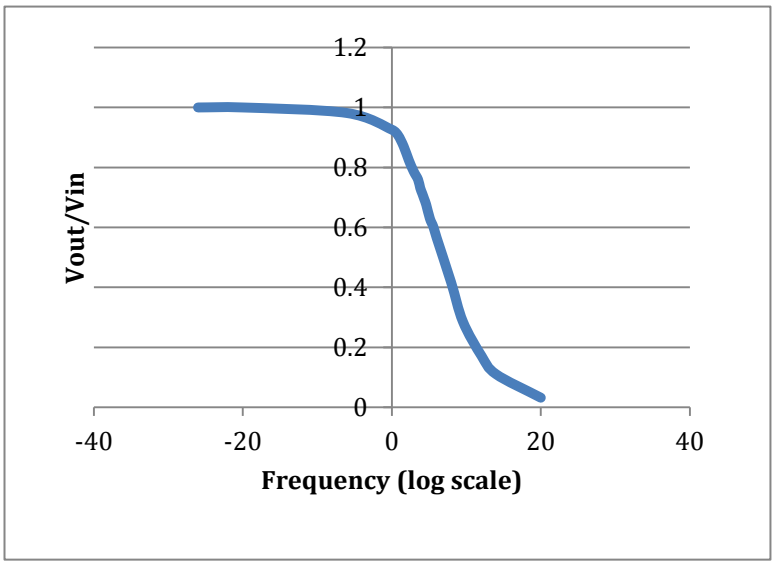
6. Construct the circuit shown below and determine its transfer characteristic and its cutoff frequency f_{3dB}. Also compare the theoretical value of f_{3dB}.



Calculation: Theoretically, we have $\omega_{3dB} = \frac{1}{\sqrt{2}RC} = 9.96krad/s$ and $f_{3dB} = \frac{\omega_{3dB}}{2\pi} \approx 1.6kHz$.

The measured results are shown below:

Frequency (kHz)	V_{in} (V)	V_{out} (V)
0.05	2.16	2.16
0.1	2.16	2.16
0.5	2.16	2.12
1	2.16	2.00
1.1	2.16	1.96
1.2	2.16	1.88
1.3	2.16	1.78
1.4	2.16	1.70
1.5	2.16	1.64
1.55	2.16	1.58
1.6	2.16	1.54
1.65	2.16	1.50
1.7	2.16	1.46
1.8	2.16	1.36
1.9	2.16	1.30
2	2.16	1.22
2.5	2.16	0.90
3	2.24	0.64
4	2.24	0.384
5	2.24	0.248
10	2.24	0.072

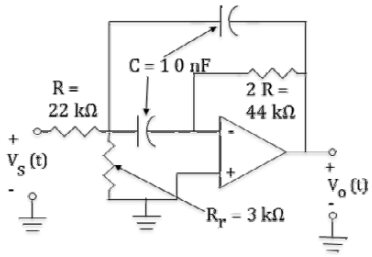


$f_{3dB} = 1.65kHz$

Conclusion: The expected cutoff frequency is $f_{3dB} = 1.6kHz$ and we get $1.65kHz$. That proves the theoretical equations. It is obvious to see that this filter is a low-pass filter.

Comparing the roll off of this low-pass filter with that of the filter in part 5, it is obviously to see this filter rolls off more sharply than that of part 5. That is, this low-pass filter is better than that of part 5.

7. Construct the circuit shown below. Determine its transfer characteristic and the center frequency f_o where the gain is at its maximum.



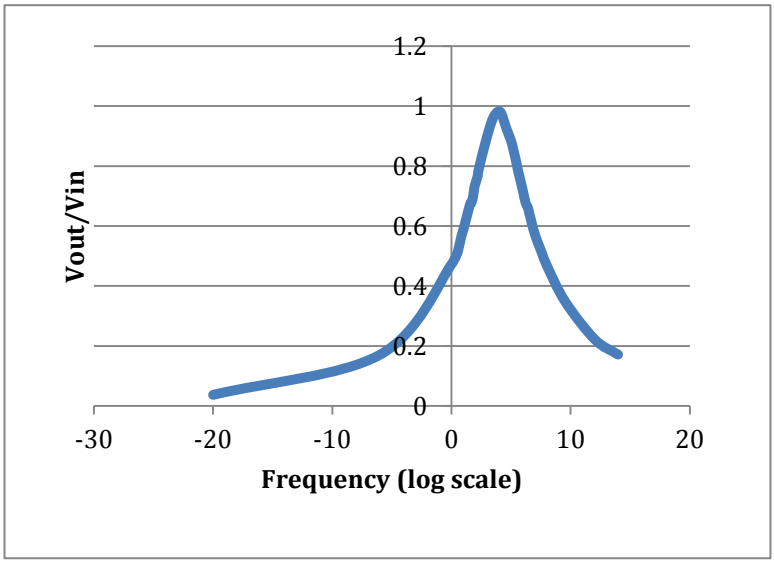
Calculation: Theoretically, the mid-band gain $H(\omega_o) = 1$ where the center frequency $\omega_o = \frac{\sqrt{1+\frac{R}{R_r}}}{\sqrt{2}RC} = \frac{\sqrt{1+22k\Omega/3k\Omega}}{\sqrt{2}\times 22k\Omega\times 10nF} \approx 9278rad/s.$

Also, the bandwidth $\Delta\omega$ should be $\frac{1}{RC} = \frac{1}{22k\Omega\times 10nF} \approx 4545.45rad/s$, and thus

$$Q = \frac{\omega_o}{\Delta\omega} = \sqrt{\frac{1+R/R_r}{2}} \approx 2.$$

The measured result is shown below (for $R = 22k\Omega$):

Frequency *(kHz)*	V_{in} *(V)*	V_{out} *(V)*
0.1	2.16	0.08
0.5	2.16	0.368
1	2.16	1.02
1.1	2.16	1.22
1.2	2.16	1.46
1.21	2.16	1.46
1.22	2.16	1.48
1.23	2.16	1.50
1.24	2.16	1.54
1.25	2.16	1.58
1.26	2.16	1.60
1.27	2.16	1.62
1.28	2.16	1.64
1.29	2.16	1.66
1.3	2.16	1.7
1.4	2.16	1.92
1.5	2.16	2.08
1.6	2.16	2.12
1.65	2.16	2.10
1.7	2.16	2.00
1.8	2.16	1.88
1.9	2.16	1.70
1.95	2.16	1.62
2	2.16	1.54
2.05	2.16	1.46
2.1	2.16	1.42
2.2	2.16	1.28
2.3	2.16	1.18
2.4	2.16	1.1
2.5	2.16	1.02
3	2.24	0.78
4	2.24	0.496
5	2.24	0.384



$f_{3dB1} = 1.24kHz$ and $f_{3dB2} = 2kHz$

so $f_o = \frac{f_{3dB1}+f_{3dB2}}{2} = 1.62kHz \Rightarrow \omega_o = 2\pi f_o = 10.18krad/s$

the bandwidth $\Delta f = 760Hz \Rightarrow \Delta\omega = 4775rad/s$

the Q-factor $Q = \frac{\omega_o}{\Delta\omega} \approx 2.13$

Conclusion: It is found that $\omega_o = 10.18krad/s$ and $\Delta\omega_o = 4775rad/s$ and $Q = 2.13$. Comparing with the theoretically values, the results reasonably prove the theoretical equations. There exist errors due to the inaccurate measurements. This

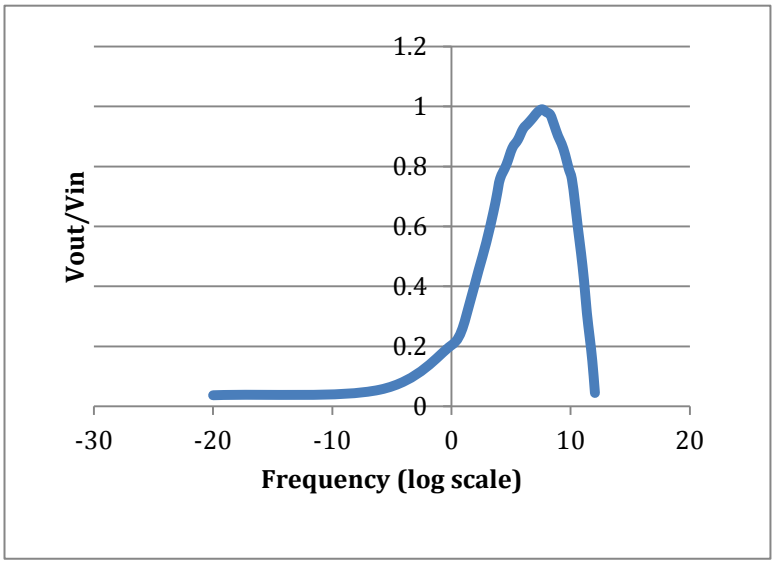
filter is a band-pass filter as we can derive from the graph.

Now if we replace $R = 22k\Omega$ with $R = 10k\Omega$, we should get the following results:

- $\omega_o = 14719.6rad/s$
- $\Delta\omega = 10krad/s$
- $Q = \frac{\omega_o}{\Delta\omega} = 1.47$

The measured result is shown below (for $R = 10k\omega$):

Frequency *(kHz)*	V_{in} *(V)*	V_{out} *(V)*
0.1	2.16	0.08
0.5	2.16	0.12
1	2.16	0.44
1.1	2.16	0.54
1.2	2.16	0.76
1.3	2.16	0.98
1.4	2.16	1.18
1.5	2.16	1.4
1.55	2.16	1.52
1.6	2.16	1.64
1.7	2.16	1.74
1.8	2.16	1.86
1.9	2.16	1.92
2	2.16	2
2.1	2.16	2.04
2.2	2.16	2.08
2.3	2.16	2.12
2.4	2.16	2.14
2.5	2.16	2.12
2.6	2.16	2.1
2.7	2.24	2.1
2.8	2.24	2.02
2.9	2.24	1.96
3	2.24	1.88
3.1	2.24	1.78
3.2	2.24	1.7
3.3	2.24	1.52
3.4	2.24	1.32
3.5	2.24	1.14
3.6	2.24	0.94
3.7	2.24	0.7
3.8	2.24	0.52



$f_{3dB1} = 1.55kHz$ and $f_{3dB2} = 3.3kHz$

so $f_o = \frac{f_{3dB1}+f_{3dB2}}{2} = 2.4kHz \Rightarrow \omega_o = 2\pi f_o = 15.24krad/s$

the bandwidth $\Delta f = 1.75kHz \Rightarrow \Delta\omega = 10.99krad/s$

the Q-factor $Q = \frac{\omega_o}{\Delta\omega} \approx 1.39$

3.9	2.24	0.34
4	2.24	0.1

Conclusion: As we vary the resistor R, in this case $R = 10k\Omega$, we will change the center frequency and bandwidth correspondingly.

Particularly, as R decreases, ω_o, $\Delta\omega$, and Q decrease but H remains. This matches what we can directly see from the theoretical equations.

Experiment #7 Feedback Amplifier

11/20&11/27

I. Abstract

Feedback amplifiers, especially negative feedback amplifiers, play an important role in system designs. This lab is designed and conducted to help students understand the characteristics of feedback amplifiers. The following four types of negative feedback amplifiers would be designed and analyzed in details: voltage amplifiers, current amplifiers, transconductance amplifiers, and transresistance amplifiers. To further understand the behaviors of compound feedback amplifiers, frequency response and stability issue of series-shunt amplifiers in series would be discussed in this report.

II. Introduction

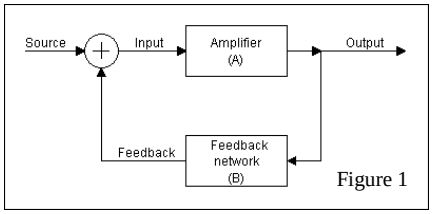


Figure 1

Most physical systems incorporate some form of feedback amplifiers. Feedback amplifiers are invented by Harold Black in 1928 (Sedra, 803). *Figure 1* shows the basic structure for a feedback amplifier. In this lab, negative feedback amplifiers are focused, as they are more useful to trade off gain for other desirable properties. Based on the quantity to be amplified (voltage or current) and the desired form of output (voltage or current), negative feedback amplifiers are classified into four categories: series-shunt, shunt-series, series-series, and shunt-shunt feedbacks. All these feedback systems have a feedback gain $A_f = \frac{A}{1+\beta A}$, where A is the open-loop gain and β is a feedback factor determined by the feedback connection.

Voltage amplifiers amplify an input voltage signal and provide an output voltage signal. This feedback topology is called "series-shunt" feedback. *Figure 2* is an example of series-shunt feedback amplifier. This amplifier results in a higher input resistance and lower output resistance. *Current amplifiers* employ the "shunt-series" feedback topology, which essentially amplifies an input current signal and provide an output current signal. The instance of this feedback amplifier is shown in *Figure 3*. This topology results in a lower input resistance and a higher output resistance. In *transconductance amplifiers*, the input signal is a voltage and the output signal is a current, and this gives that the feedback topology is "series-series" feedback. An example is shown in *Figure 4*. This provides the amplifier with both higher input and output resistances.

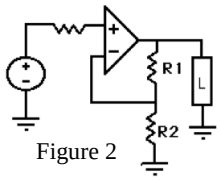


Figure 2

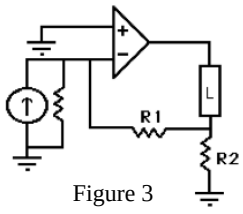


Figure 3

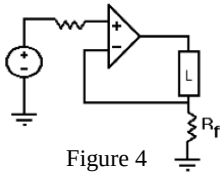


Figure 4

Finally, *transresistance amplifiers*, shown in *Figure 5*, amplify an input current and provide an output voltage signal. This kind of amplifier is also known as "shunt-shunt" feedback amplifiers. It results in both lower input and output resistances.

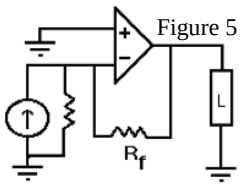


Figure 5

In this experiment, part 1 through 4 demonstrate the design, implementation, and test of these four types of negative feedback amplifiers implemented with the regular amplifier LM741. *Figure 6* shows the LM741 layout from Intersil. From the datasheet, the open-loop gain for the IC model LM741 at supply voltage $18V$ is around 107 in dB. This tells $A \approx 10^{107/20} = 2.24 \times 10^5$. Since the feedback gain $A_f = \frac{A}{1+\beta A}$, as A is this large, it is reasonable to assume that $A_f \approx 1/\beta$.

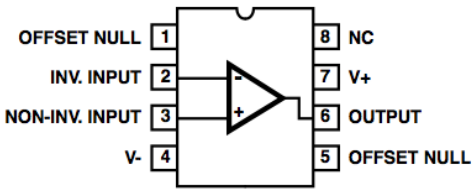


Figure 6

Part 5 emphasizes the frequency response of a cascaded feedback circuit. Moreover, part 6 and 7 are done in PSpice to explore the stability issue and the method of compensation.

III. Experiment Details and Results

Part 1: Series-Shunt Feedback

The goal is to design a series-shunt negative feedback amplifier (*Figure 7*) that has a no-load voltage gain of about $15V/V$. Then determine the low-frequency small-signal input resistance and the location of the dominant pole in the sinusoidal steady state response.

The feedback factor β for this configuration can be seen as: $\beta = \frac{V_1}{V_2}\Big|_{I_1=0} = \frac{R_2}{R_1+R_2}$. As it is discussed in the end of section II, we see $A_f \approx \frac{1}{\beta} = 15 \Rightarrow \beta = \frac{R_2}{R_1+R_2} = \frac{1}{15}$. From this, it is not hard to find the relation that $R_1/R_2 = 14$. Choose $R_1 = 14k\Omega$ and $R_2 = 1k\Omega$. In the circuit, R_s is estimated to be $1M\Omega$ for the input source resistance.

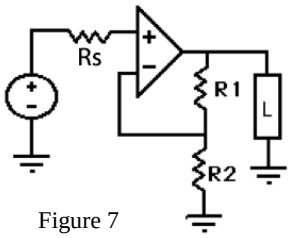


Figure 7

Construct the circuit and set the supply voltage to be $18V$ to meet the large open loop gain A specification for LM741. Then the experimental results are shown below.

R_{Load} $(k\Omega)$	V_{out} (V)	V_{in} (V)	A_f (V/V)
∞	16.6	1.12	14.82
10	16.4	1.10	14.91
5.1	16.4	1.10	14.91
2.2	16.4	1.10	14.91

The measured $A_f \approx 15V/V$. It meets the expected value.

The input resistance is measured by the method of test voltage. Replace the source voltage and the estimated source input resistance with a DC test voltage V_{test}. Measure the current I_{test} going into the positive "+" end of the amplifier, and then the input resistance R_{if} should be V_{test}/I_{test}. It turns out that $V_{test} = 18V$ and $I_{test} = 36.2\mu A$. Hence, $R_{if} \approx 497.24k\Omega$.

Last but not least, the dominant pole in the open loop response should be determined by $f_p = \frac{f_{3dB}}{1+A\beta}$, where f_{3dB} indicates the cutoff frequency, which is also known as the dominant pole in the sinusoidal steady state response. f_{3dB} is measured by applying different frequencies to the circuit as shown in *Figure 7* and find when V_o turns to be $V_{o_{max}}/\sqrt{2}$. Theoretically, $\frac{V_o}{\sqrt{2}} \approx 11.6V$ for $V_o = 16.4V$. The result is shown in the table below.

Applied f (kHz)	10	15	20	25	30	35	40
V_{in} (V)	1.10	1.10	1.10	1.10	1.10	1.10	1.10
V_{out} (V)	16.4	16.0	15.6	14.4	11.8	8.6	4.2

Hence, it has been found that the dominant pole in the sinusoidal steady state response is $f_{3dB} = 30kHz$. The dominant pole in the open loop response is then $f_p = \frac{30kHz}{1+2.24\times10^5\times\frac{1}{15}} = 2.01Hz$.

Part 2: Shunt-Series Feedback

The goal is to design a shunt-series negative feedback amplifier (*Figure 8*) that has a no-load voltage gain of about $100A/A$.

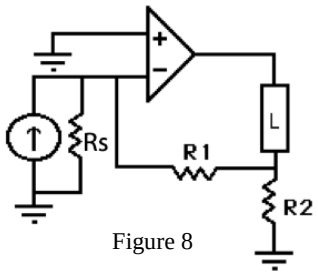


Figure 8

The feedback factor β for this configuration can be seen as: $\beta = \frac{I_1}{I_2}\Big|_{V_1=0} = \frac{R_2}{R_1+R_2}$. As it is discussed in the end of section II, we see $A_f \approx \frac{1}{\beta} = 100 \Rightarrow \beta = \frac{R_2}{R_1+R_2} = \frac{1}{100}$. It is reasonable to choose $R_1 = 100k\Omega$ and $R_2 = 1k\Omega$ since $R_1 \gg R_2$. This assumption makes $A_f = 101A/A$. In the circuit, R_s is estimated to be $1M\Omega$ for the input source resistance.

Construct the circuit and the results are shown below.

R_{Load} $(k\Omega)$	I_{out} (μA)	I_{in} (μA)	A_f (A/A)
∞	497	5	99.4
10	503	5	100.6
5.1	508	5	101.6
2.2	512	5	102.4

The result matches the theoretical estimation.

Part 3: Series-Series Feedback

The goal is to design a series-series negative feedback amplifier (*Figure 9*) that has a no-load voltage gain of about $1mA/V$. The feedback factor β for this configuration can be

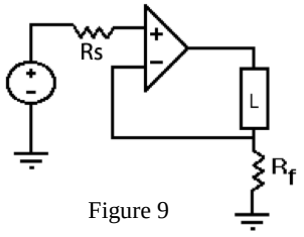


Figure 9

seen as: $\beta = \frac{V_1}{I_2}\Big|_{I_1=0} = R_f$. As it is discussed in the end of section II, we see $A_f \approx \frac{1}{\beta} = 10^{-3} A/V \Rightarrow \beta = R_f = 1/10^{-3}$. Thus $R_f = 1k\Omega$. In the circuit, R_s is estimated to be $1M\Omega$ for the input source resistance.

Construct the circuit and the measurements are shown in the table below.

R_{Load} $(k\Omega)$	I_{out} (mA)	V_{in} (V)	A_f (mA/V)
∞	1.1	1.12	0.982
10	1.16	1.12	1.036
5.1	1.14	1.12	1.018
2.2	1.1	1.12	0.982

The result meets the expectation.

Part 4: Shunt-Shunt Feedback

The goal is to design a shunt-shunt negative feedback amplifier (*Figure 10*) that has a no-load voltage gain of about $100k\Omega$. The feedback factor β for this configuration can be seen as: $\beta = \frac{I_1}{V_2}\Big|_{V_1=0} = \frac{1}{R_f}$. As it is discussed in the end of section II, we see $A_f \approx \frac{1}{\beta} = 100k\Omega \Rightarrow \beta = R_f = 100k\Omega$. In the circuit, R_s is estimated to be $1M\Omega$ for the input source resistance.

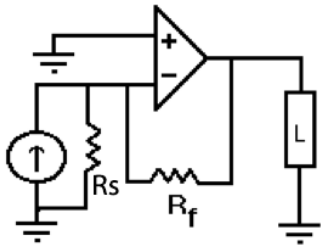


Figure 10

Construct the circuit and the measurements are shown in the table below.

R_{Load} $(k\Omega)$	V_{out} (mV)	I_{in} (μA)	A_f $(k\Omega)$
∞	512	5	102.4
10	508	5	101.6
5.1	508	5	101.6
2.2	504	5	100.8

The result meets the expectation.

Part 5: Frequency Response

The goal is to measure the frequency response and determine the Q of the compound amplifier (*Figure11*) using two of the amplifier in part 1. The required overall voltage gain should be around 15 at mid-band.

The DC offset voltage of the first op amp is amplified by the second op amp. This procedure might cause saturation during experiment. Thus it is required to use a trimmer (variable resistor) to adjust the offset of the first op amp. To do this, first

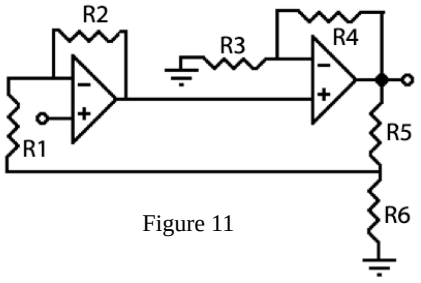


Figure 11

construct the circuit shown in *Figure 12*. Change the resistance of the trimmer until V_o reaches 0. Then the offset would be set to 0 to prevent saturation. After this is done, construct the circuit shown in *Figure 11*. Since the overall gain is required to be 15, it is verified in PSpice that $R_1 = R_3 = R_6 = 1k\Omega$ and $R_2 = R_4 = R_5 = 14k\Omega$ should give a gain of 15. The measured result is below.

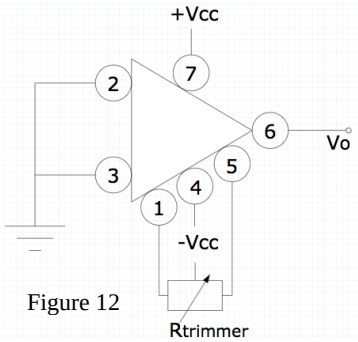
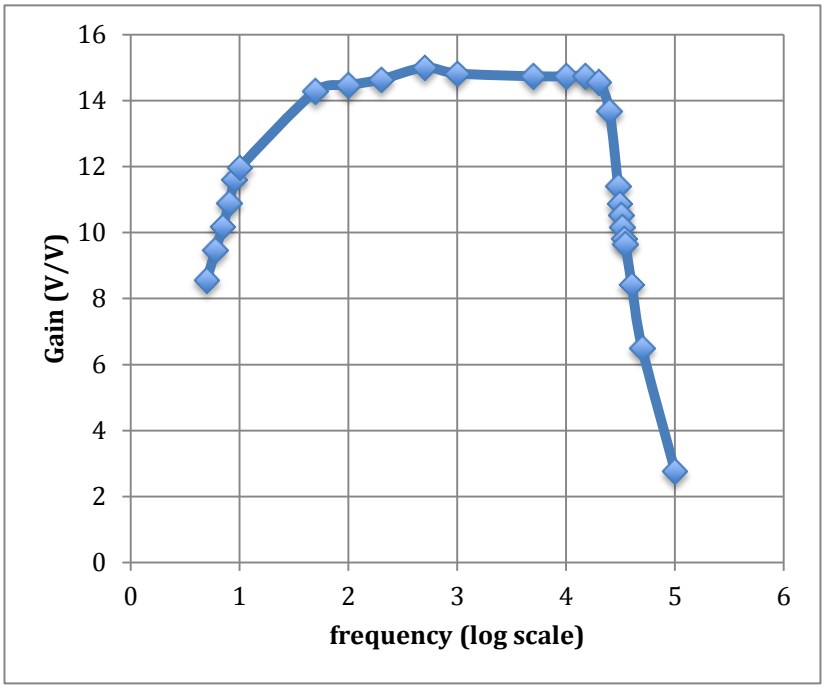


Figure 12

f (kHz)	v_{in} (V)	v_{out} (V)
0.005	1.12	9.6
0.006	1.12	10.6
0.007	1.12	11.4
0.008	1.12	12.2
0.009	1.12	13
0.01	1.12	13.4
0.05	1.12	16
0.1	1.12	16.2
0.2	1.12	16.4
0.5	1.12	16.8
1	1.12	16.6
5	1.14	16.8
10	1.14	16.8
15	1.14	16.8
20	1.14	16.6
25	1.14	15.6
30	1.14	13
31	1.14	12.4
32	1.14	12
33	1.14	11.6
34	1.14	11.2
35	1.14	11
40	1.14	9.6
50	1.14	7.4
100	1.14	3.16



$f_{3dB_1} \approx 7Hz$ and $f_{3dB_2} \approx 32kHz$

As it is measured, the cutoff frequency f_{3dB}s are $7Hz$ and $32kHz$, roughly behaves as a bandpass filter. It is discovered that the frequency $f = \frac{f_{3dB_1} + f_{3dB_2}}{2} \approx 16kHz$ and the bandwidth is about $32kHz$. The Q-point is calculated by $\frac{\Delta f}{f} = \frac{32kHz}{16kHz} = 2$.

The output for input square waves is examined by various frequencies in the table below.

f (kHz)	1	5	10	50	60	80	100
v_{in} (V)	1.20	1.20	1.20	1.34	1.34	1.34	1.34
v_{out} (V)	18	19.6	20.2	20.6	18.76	13.60	4.08

As frequency goes higher and higher, the output wave gradually turns to be a triangular waveform. The example is shown in *Figure 13*.

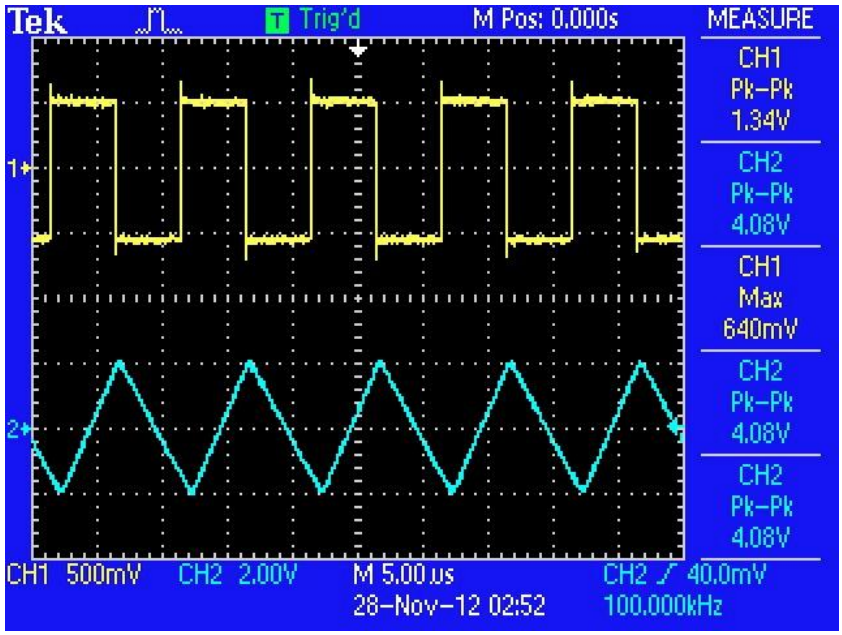


Figure 13

Part 6: Stability

The goal of this part is to investigate the stability of the compound amplifier with three amplifiers designed in part 1. PSpice is employed in this part. The overall feedback should be variable from 10 to 100. The designed schematic is shown in *Figure 14*.

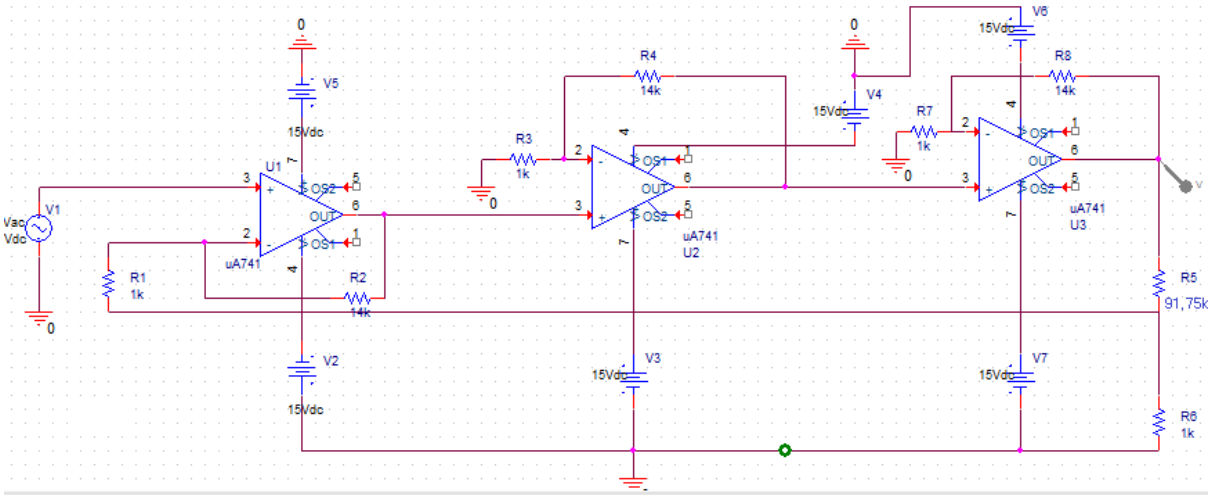


Figure 14

The parameters in the circuit is shown below:

- $R_1 = R_3 = R_6 = R_7 = 1k\Omega$
- $R_2 = R_4 = R_8 = 14k\Omega$
- For the overall gain to be in the range $[10, 100]$, it is investigated that $R_5 \in [7.865k\Omega, 91.75k\Omega]$.

Figure 15 and *Figure 16* present the magnitudes of the output when the overall gain is 10 ($R_5 = 7.865k\Omega$)and when the overall gain is 100 ($91.75k\Omega$), respectively.

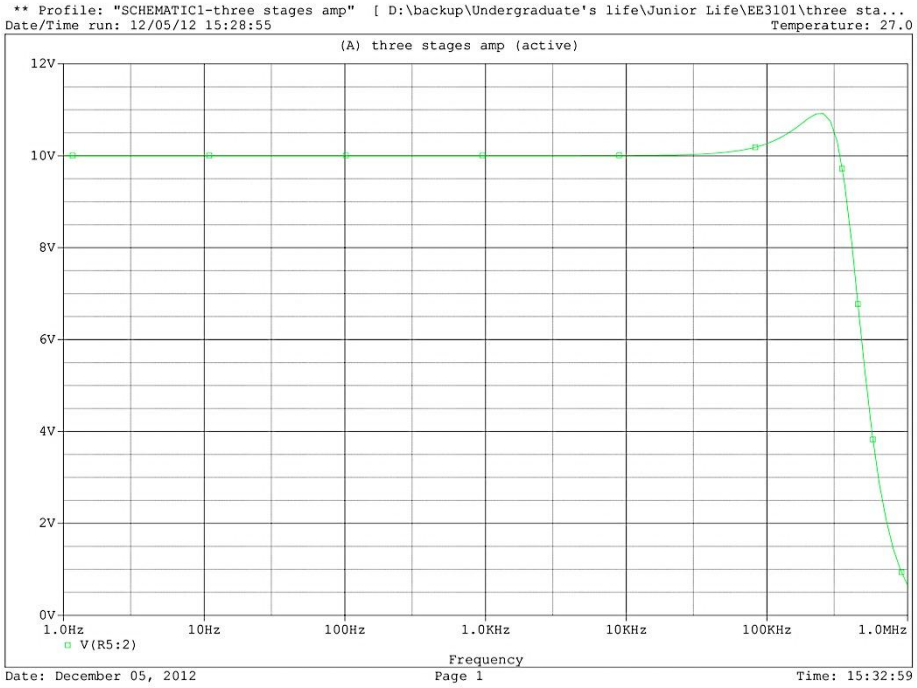


Figure 15

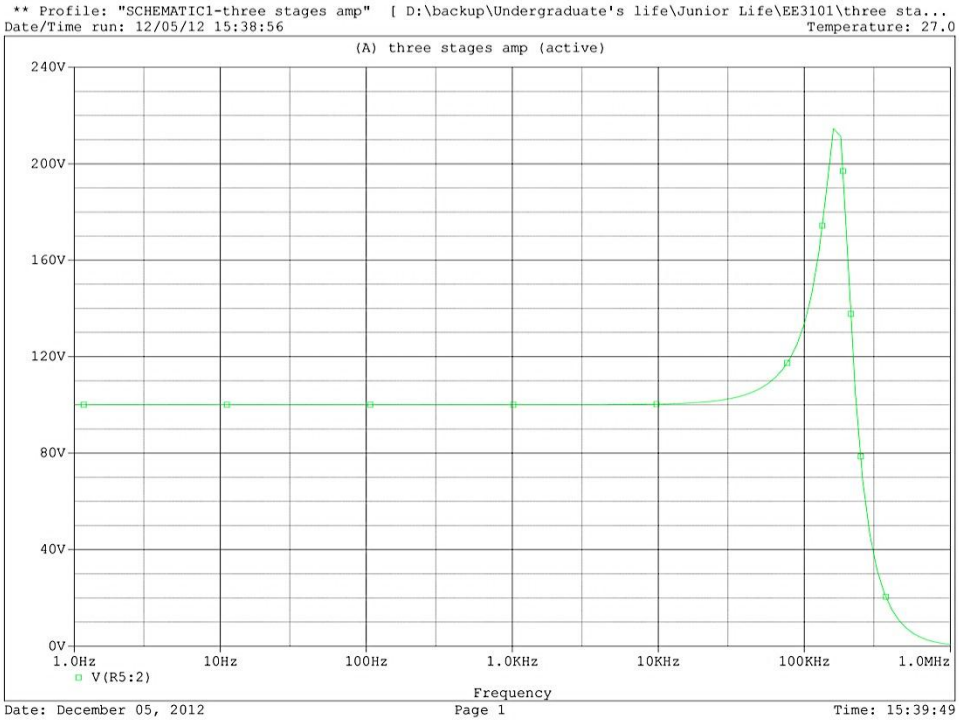


Figure 16

From the figures, the larger the gain is, the more the amplifier becomes unstable.

Part 7: Compensation

The goal for this part is to determine a dominant pole compensation to give stability with a phase margin between 45° and 90°. Here the circuit that has a gain equals $100V/V$ is chosen to be compensated.

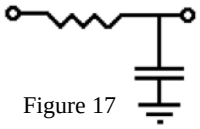


Figure 17

The compensation can be done to insert the network shown in *Figure 17* between stages. From the uncompensated bode plots for magnitude (*Figure 18 lower part*) and phase diagram (*Figure 18 upper part*) of the circuit, it is observed that the frequency to allow a stability is ranged from $170kHz$ to $260kHz$ between 45° and 90°. A detailed phase diagram is shown in *Figure 19* to help determine the values derived above.

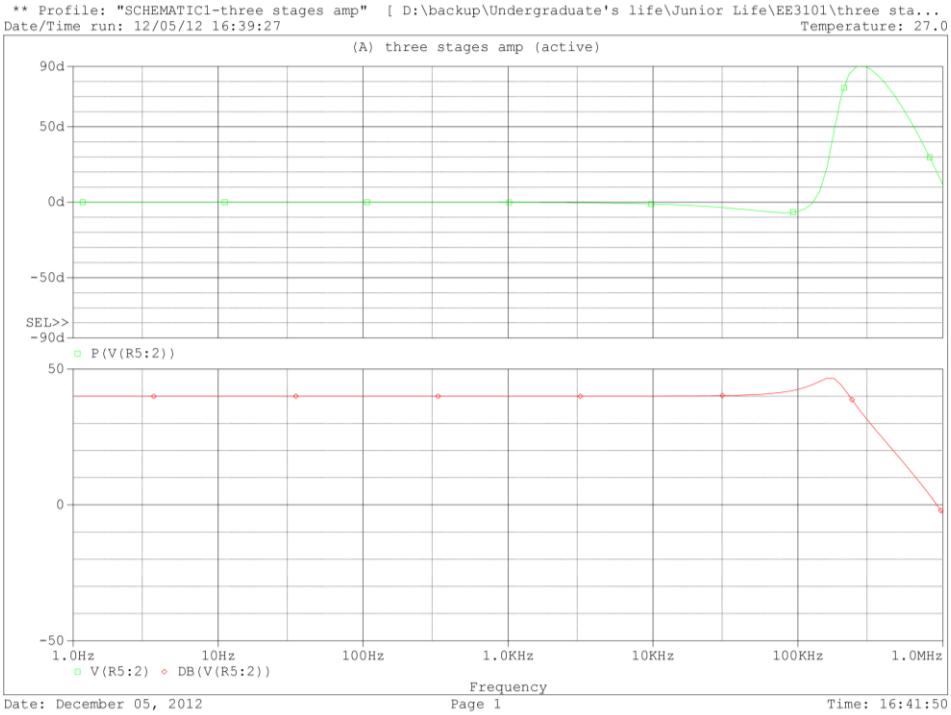


Figure 18

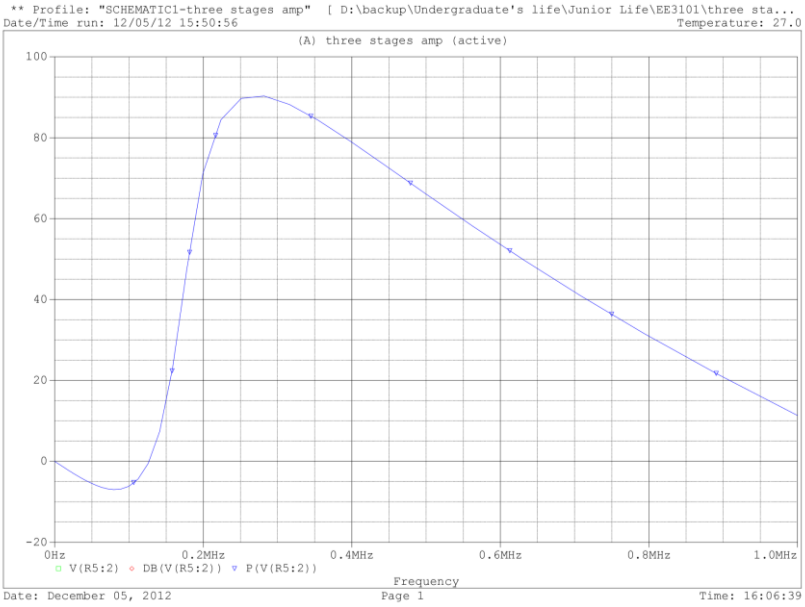


Figure 19

So it is reasonable to choose the pole where $f = 170kHz$ to start a compensation.

Since we have $40dB$ for the magnitude and there's $20dB/decade$ for a pole, the pole we want to add should be at $f_D = 1.7kHz$. Since $\omega_o = \frac{1}{RC} = 2\pi f_o$, the relation between RC can be derived that $RC \approx 9.362 \times 10^{-5}$. Choose $R = 93.62k\Omega$ and $C = 1nF$ would satisfy this relation.

Then the modified circuit is shown below in *Figure 20* and the compensated bode plots for magnitude (*Figure 21 lower part*) and phase diagram (*Figure 21 upper part*) of the circuit.

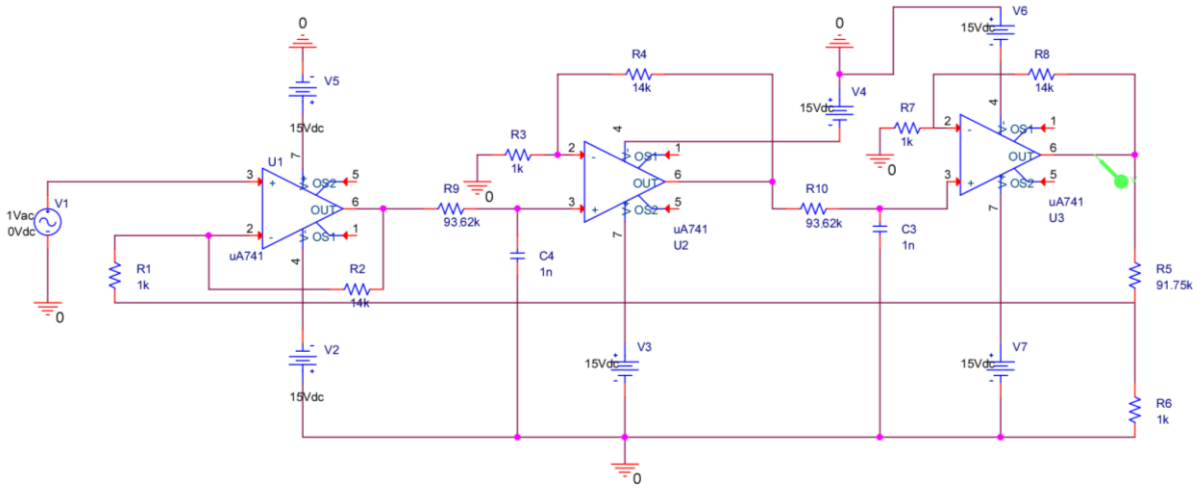


Figure 20

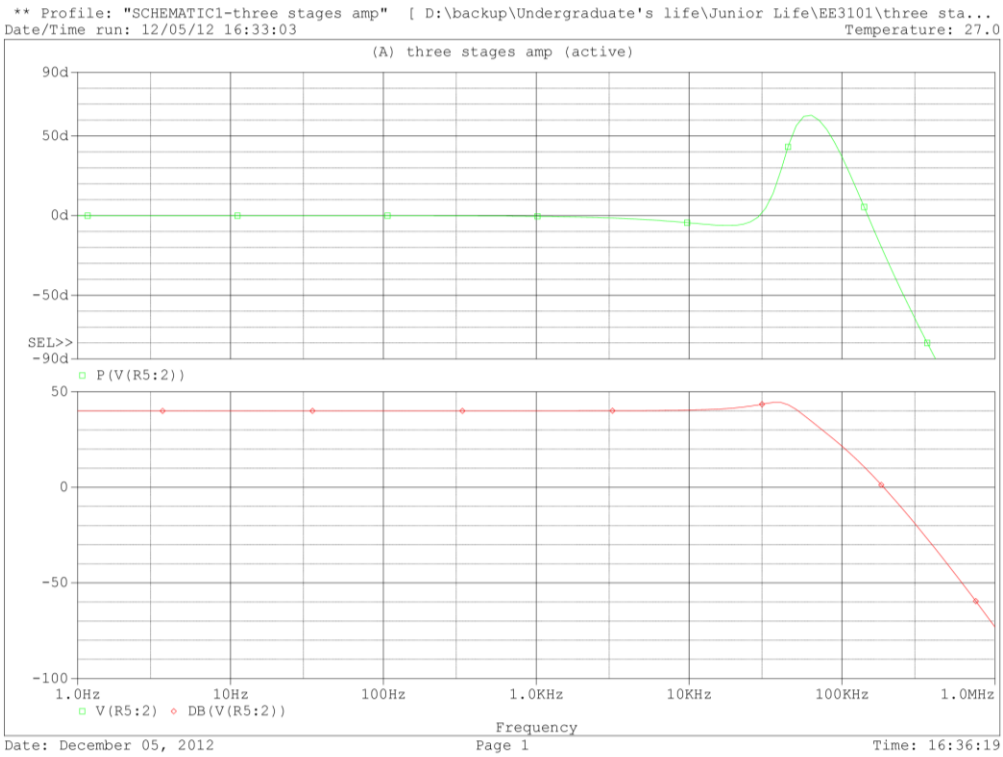


Figure 21

Compare *Figure 18* and *Figure 21*, it is clear to see the compensated amplifier turns to be stable since we have changed the dominant pole to be $f_D = 1.7kHz$.

IV. Conclusion

This experiments guide the students to understand basic behaviors of four categories of feedback networks in amplifier designs. The close loop gain of different circuits is verified one by one through experiments. Moreover, compound amplifiers are discussed. Stability issues and the method to compensation are also explored in compound amplifiers. The criteria designed and the theoretical values are matched and under expectation. As two or more amplifiers are connected, instability of the whole system arises. The compensation turns to be the solution to make the system stable and functional. Since the stability and compensation are done in PSpice, which is basically a simulation, it is not sure how large the efficiency could be in reality.

V. Reference

EE 3101 Lab Manual.

Intersil. *LM741 Datasheet*.

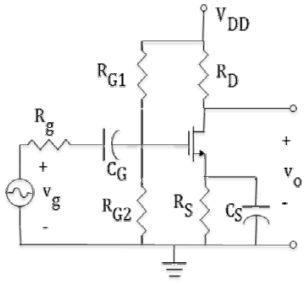
Basic Feedback Amplifier. Digital image. *Study Villa*. N.p., n.d. Web. <http://www.studyvilla.com/feedback.aspx>

Sedra, Adel S., and Kenneth Carless. Smith. *Microelectronic Circuits*. 6th Ed. New York: Oxford UP, 2009. Print.

Experiment #5 High Frequency Behavior of MOSFET

12/04

1. *Construct the common source amplifier with MOSFET type 2N7000 shown below. Find the transconductance* g_m *at midband frequencies and the midband gain* V_o/V_i.



The following specs are required:

- $I_D = 2mA$
- $V_{DC} = 8V$
- $R_g = 5k\Omega$
- $R_D = R_S$
- $V_{DD} = 16V$

Calculation: It is obvious to derive $V_{DD} - V_{DC} = I_D(R_D + R_S)$. Since $I_D = 2mA$, $V_{DC} = 8V$, and $V_{DD} = 16V$, we can find $R_D = R_S = 2k\Omega$.

Since $V_{GS} - V_t = V_{OV}$, we have $I_D = \frac{1}{2} g_m V_{OV} = \frac{1}{2} g_m (V_{GS} - V_t)$.

To find g_m, it is required to know V_t and measure I_D and V_{GS}. Unfortunately the only information is "V_t is small compare to V_{GS} so the MOSFET can be in the active mode". Hence, it is reasonable to do a few measurements to find out the values.

Construct the circuit without v_g, R_g, C_G, and C_S first. Vary values for R_{G1} and R_{G2} and measure V_{GS} and I_D. Indeed, V_{GS} should be a fairly large number compare to V_t.

The result is shown below:

I_D (mA)	V_{GS} (V)	R_{G1} $(M\Omega)$	R_{G2} $(M\Omega)$
2.837	2.326	1	1
3.997	2.673	1	2
1.534	2.265	2	1

So we derived: $\begin{cases} 2.837 = \frac{1}{2} g_m (2.326 - V_t) \\ 3.997 = \frac{1}{2} g_m (2.673 - V_t) \\ 1.534 = \frac{1}{2} g_m (2.265 - V_t) \end{cases}$. Then solve for g_m and V_t, it is reasonable to conclude that $g_m \approx 12.6mA/V$ and $V_t \approx 1.8841V$ to best satisfy the three group of values.

To achieve $I_D = 2mA$, thus we have $2 = \frac{1}{2} \times 12.6 \times (V_{GS} - 1.8841) \Rightarrow V_{GS} \approx 2.2V$ and thus $V_G = 6.4V$. This tells $R_{G1}/R_{G2} \approx 1.5$. Here $R_{G1} = 150k\Omega$ and $R_{G2} = 100k\Omega$ are picked. Correspondingly, $R_{in} = 60k\Omega$.

Insert v_g, R_g, C_G, and C_S back. Since it is required that C_G and C_G have to be chosen so as to maintain the high input impedance, it is reasonable to choose the largest capacitors we have. In

the lab kit, there are two $10\mu F$ capacitors and one $47\mu F$ capacitor can be employed. Here it is chosen that $C_G = 10\mu F$ and $C_S = 47\mu F$. Also $R_g = 5k\Omega$ and the input voltage source is chosen to be $0.05V$ peak value. And then it is measured that at $V_{in} = 0.1V$, $V_o = 2.46V$.

Conclusion: It is reasonable to conclude that $g_m \approx 12.6mA/V$ and $V_t \approx 1.8841V$. The midband gain is $A_m = \frac{V_o}{V_{in}} = 24.6V/V$ regarding to the measured results. Theoretically, we have $A_m = g_m \frac{R_{in}}{R_{in}+R_g}(R_D \parallel r_o) \approx g_m R_D \frac{R_{in}}{R_{in}+R_g}$, which gives $A_m \approx 23.2615V/V$. One possible explanation is r_o is not that large to be ignored. In this case, $r_o \approx 34.76k\Omega$.

2. *Measure the high frequency $3dB$ down f_H circuit designed in part 1.*

Calculation: $f_H = \frac{1}{2\pi(R_g \parallel R_{in})\left(C_{gs}+C_{gd}(1+g_m R_D)\right)} = \frac{1}{2\pi(5k\Omega \parallel 60k\Omega)\left(C_{gs}+C_{gd}(1+12.6R_D)\right)}$.

It is measured that at $f_H = 89kHz$, $V = 1.74V \approx 2.46 \times 0.707V$.

Conclusion: One equation is derived for C_{gs} and C_{gd}: $89 \times 10^3 = \frac{1}{28.9993(C_{gs}+26.2C_{gd})}$

3. *Now measure f_H again with $R_D = 1k\Omega$.*

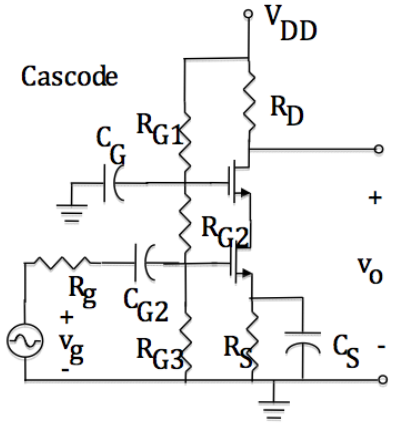
It is measured that at $f_H = 120kHz$, $V = 1.72\square \approx 2.46 \times 0.707V$.

Conclusion: Another equation is derived for C_{gs} and C_{gd}: $120 \times 10^3 = \frac{1}{28.9993(C_{gs}+13.6C_{gd})}$.

4. *Solve for the equations and determine the value of C_{gs} and C_{gd}.*

Calculation: $\begin{cases} 89 \times 10^3 = \frac{1}{28.9993(C_{gs}+26.2C_{gd})} \\ 120 \times 10^3 = \frac{1}{28.9993(C_{gs}+13.6C_{gd})} \end{cases} \Rightarrow \begin{cases} C_{gs} = 179.33nF \\ C_{gd} = 7.9439nF \end{cases}$.

5. Build a cascade amplifier using the figure below as a guide. Measure the gain and bandwidth of this circuit and compare with the values obtained earlier.



It is required that $I_D = 2mA$ and $R_S = R_D$. Also C_G, C_D, R_S, R_D, and R_g should be chosen as same as they are chosen in part 1.

Calculation: $I_D = 2mA \Rightarrow R_D = R_S = 2k\Omega$ following the same procedure in part 1.

We have $g_m \approx 12.6mA/V$ and $V_t \approx 1.8841V$. We should know that $I_D = \frac{1}{2}g_m V_{OV} \Rightarrow V_{OV} = 0.3175V \Rightarrow V_{GS1} = V_{GS2} = 2.2V$. So $V_{G3} = 6.2V$ and

theoretically $V_{G2} = V_{GS1} + V_{DS2} + I_D R_S \approx 10.2V$.

The designed circuit has the specs listed below:

- $C_G = C_{G2} = 10\mu F,\ C_S = 47\mu F$
- $R_D = R_S = 2k\Omega$
- $R_g = 5k\Omega$

It is investigated in the circuit that $R_{G1} = R_{G2} = 1M\Omega$ and $R_{G3} = 1.3M\Omega$ would give closer values for the required voltage divider and achieve $I_D = 2.02mA \approx 2mA$.

Construct the circuit and measure the gain. It is found that the peak output voltage $v_o = 552mV$ at $6kHz$ with the input source $112mV$.

The cutoff should occur at $552mV \times 0.707 \approx 390.26mV$. It is not hard to see from the oscilloscope that at both $f_{c1} = 410kHz$ and $f_{c2} = 52Hz$, the output voltage $v_o = 392mV$.

Conclusion: From the measured results, the midband gain of this cascade amplifier is about $4.9286V/V$. Also, it can be calculated that the bandwidth is $f_{c1} - f_{c2} = 409.948kHz$. It is seen that the midband gain of this cascade amplifier is much smaller than that in the first part of this experiment due to the cascade MOSFETs.

The End